



Hi3521/Hi3520A Hardware Design **User Guide**

Issue	03
Date	2012-11-30

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About This Document

Purpose

This document describes the design recommendations for the hardware principle diagrams, printed circuit board (PCB), and board heat dissipation of the Hi3521.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3521	V100
Hi3520A	V100

Intended Audience

This document is intended for:

- Technical support personnel
- Board development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 03 (2012-11-30)

This issue is the third official release, which incorporates the following changes:

Chapter 3 Design Recommendations for the Board Heat Dissipation

In section 3.1, the descriptions are updated.



Issue 02 (2012-09-21)

This issue is the second official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

In section 1.1.2, the requirement on the connection mode of the WDG_RSTN and RSTN pin is added.

In section 1.1.5, Figure 1-4 and Figure 1-5 are updated, and the requirements on the ferrite beads for isolating the DVDD10 and DVDD33 pins of the chip and the PLL power pins are added.

In section 1.2.1.2, Figure 1-9 "Connection mode of the DDR_PADLO, DDR_PADHI, and DDR_RTT pins" is added.

In sections 1.2.4 and 1.2.7, the descriptions are updated.

Chapter 2 PCB Design Recommendations

In section 2.3.1, the descriptions of decoupling capacitors are updated.

In section 2.3.2, the requirement on the VREF pin length is updated.

In sections 2.3 and 2.4, the design recommendations are updated.

In section 2.6, the impedance of the differential trace is updated.

Issue 01 (2012-08-30)

This issue is the first official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

In section 1.1.5, the sentence "The DC-DC chip with 5 A or larger power supply capability is recommended", Figure 1-4, and Figure 1-5 are added.

In section 1.2.1.3, the descriptions above Figure 1-13 are updated, and Figure 1-15 is added.

In section 1.2.9, the last note is added.

In section 1.2.10, Table 1-6 is added.

Chapter 2 PCB Design Recommendations

In section 2.3.2, the PCB design recommendations are updated.

In section 2.10, the descriptions are updated, and Table 2-1 is added.

Chapter 3 Design Recommendations for the Board Heat Dissipation

In section 3.2, the descriptions of heat dissipation for the Hi3521 are updated.

Issue 00B10 (2012-06-30)

This issue is the sixth draft release, which incorporates the following changes:

Chapter 2 PCB Design Recommendations

Section 2.10 is added.



Issue 00B05 (2012-06-08)

This issue is the fifth draft release, which incorporates the following changes:

Chapter 2 PCB Design Recommendations

In section 2.2, the capacitor quantity is changed, and the requirements on the layout of the capacitors for the 1V0_Core power and 1.5 V power are added.

In section 2.10, a requirement is added if the minimum system design for the Hi3521 demo board is not applicable.

Issue 00B04 (2012-05-16)

This issue is the fourth draft release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

In section 1.1.5, the descriptions are updated.

Chapter 2 PCB Design Recommendations

In section 2.1, the descriptions are updated.

Section 2.2 "Design Recommendations for the Core Power Area" is added.

In section 2.10, recommendation 1 is added.

Chapter 3 Design Recommendations for the Board Heat Dissipation

This chapter is added.

Issue 00B03 (2012-04-20)

This issue is the third draft release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

This chapter is added.

Issue 00B02 (2012-03-29)

This issue is the second draft release, which incorporates the following changes:

Chapter 2 PCB Design Recommendations

The descriptions are updated.

Issue 00B01 (2012-03-20)

This issue is the first draft release.



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1 Design Recommendations for Schematic Diagrams

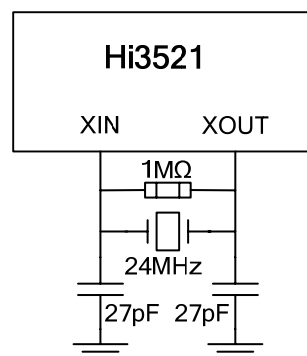
1.1 Requirements on the External Circuits of the Minimum System

1.1.1 Clocking Circuit

The system clock circuits can be designed in either of the following ways:

- Combines the internal feedback circuit of the Hi3532 with an external 24 MHz crystal oscillator circuit. [Figure 1-1](#) shows the recommended connection mode of the crystal oscillators and the component specifications.
- Generates clocks by using the external clock circuit and input clocks over the XIN pin.

Figure 1-1 Recommended connection mode of the crystal oscillator and component specifications



1.1.2 Reset and Watchdog Circuit

The Hi3521 RSTN pin is a reset signal input pin. The valid reset signal must have low-level pulse and the pulse width must be greater than 12 cycles of the crystal oscillator clock input from the XIN pin. The pulse width of the reset signal is 100–300 ms in general.

During the board-based design, you are advised to use a dedicated reset chip to generate reset signals to ensure system stability. If an exception occurs when the Hi3521 is reset, the Hi3521



can generate low-level pulses through the WDG_RSTN pin. Therefore, the WDG_RSTN pin can be connected to the input pin of the system reset chip to reset the entire system.

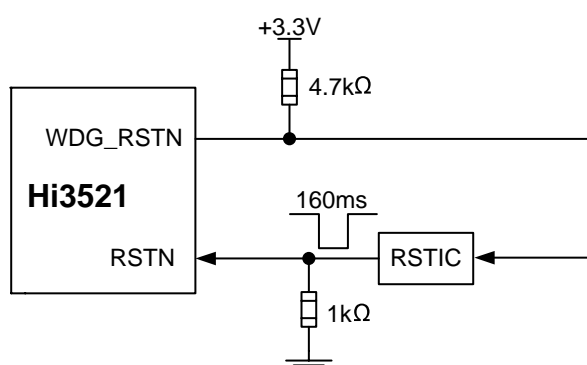


CAUTION

The WDG_RSTN pin is open drain (OD) output and must be connected to an external pull-up resistor. The WDG_RSTN cannot connect directly to the RSTN pin.

Figure 1-2 shows the typical reset and watchdog circuit.

Figure 1-2 Typical reset and watchdog circuit



1.1.3 JTAG Debug Interface

The Hi3521 Joint Test Action Group (JTAG) interface complies with the IEEE1149.1 standard. The PC can connect to the Realview-ICE simulator over this interface. Table 1-1 describes the signals of the JTAG debug interface.

Table 1-1 Signals of the JTAG debug interface

Signal	Signal Description
TCK	JTAG clock input, internal pull-down. You are advised to connect a pull-down resistor on the board.
TDI	JTAG data input, internal pull-up. You are advised to connect a pull-up resistor on the board.
TMS	JTAG mode select input, internal pull-up. You are advised to connect a pull-up resistor on the board.
TRSTN	JTAG reset input, internal pull-down. When the Hi3521 works properly, you are advised to connect a pull-down resistor on the board.
TDO	JTAG data output. You are advised to connect a pull-up resistor on the board.



NOTE

For details about the impedance of the external pull-up resistors and pull-down resistors, see [Figure 1-3](#).

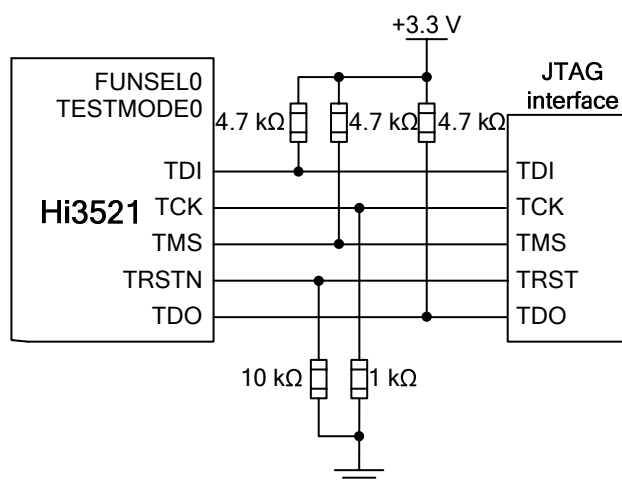
You can set the operating mode of the Hi3521 to normal mode or test mode by configuring the TEST_MODE pin. In normal mode, a 10 kΩ pull-down resistor is used. For details, see [Table 1-2](#).

Table 1-2 Description of the TEST_MODE pin

TEST_MODE	Description
0	The Hi3521 works in normal mode.
1	The Hi3521 works in test mode. In this case, the design for test (DFT) or board interconnection test can be performed.

[Figure 1-3](#) shows the JTAG connection mode and standard connector pins.

Figure 1-3 JTAG connection mode and standard connector pins



1.1.4 System Configuration Circuit for Hardware Initialization

The Hi3521 has an embedded A9 CPU and can boot from the serial peripheral interface (SPI) flash, NAND flash or double-data rate (DDR). The NAND flashes with various specifications are supported. Therefore, hardware needs to be configured as required during Hi3521 hardware initialization. You can implement the configurations in [Table 1-3](#) by connecting pull-up resistors and pull-down resistors on the board.

[Table 1-3](#) describes hardware configuration signals.

Table 1-3 Signal Description

Signal	Direction	Description
JTAG_SEL0/JTAG_SEL	I	JTAG debug select.



Signal	Direction	Description
1 (Note: These two pins are multiplexed with other functional pins.)		The values of JTAG_SEL 1or JTAG_SEL 0 are as follows: 00: A9 debug 01: reserved 10: SATA 11: reserved
BOOTSEL0/BOOTSEL1	I	BOOTSEL0 works with BOOTSEL1. The two signals indicate the boot mode select. The values of BOOTSEL1 or BOOTSEL0 are as follows: 00: boot from the SPI NOR flash 01: reserved 10: boot from the NAND flash 11: BOOTROOM
NF_BOOT_PIN[4:0]	I	NAND flash parameter setting select. 00001: 2 KB page size, 1-bit ECC, 64 pages/blocks, 5 addresses 00011: 2 KB page size, 4-bit ECC, 64 pages/blocks, 5 addresses 00101: 2 KB page size, 24-bit ECC, 64 pages/blocks, 5 addresses 00110: 2 KB page size, 1-bit ECC, 64 pages/blocks, 4 addresses 01000: 4 KB page size, 4-bit ECC, 128 pages/blocks, 5 addresses 01001: 4 KB page size, 4-bit ECC, 64 pages/blocks, 5 addresses 01010: 2 KB page size, 4-bit ECC, 64 pages/blocks, 4 addresses 01011: 4 KB page size, 24-bit ECC, 128 pages/blocks, 5 addresses 01101: 8 KB page size, 24-bit ECC, 128 pages/blocks, 5 addresses 10000: 8 KB page size, 24-bit ECC, 64 pages/blocks, 5 addresses 10001: 4 KB page size, 24-bit ECC, 64 pages/blocks, 5 addresses 10011: 4 KB page size, 1-bit ECC, 64 pages/blocks, 5 addresses 10101: 2 KB page size, 4-bit ECC, 128 pages/blocks, 5 addresses 11001: 2 KB page size, 24-bit ECC, 128 pages/blocks, 5 addresses



1.1.5 Power Supply Circuit

For details about the requirements on the power supplies of the Hi3521, see the "Electrical Specifications" sections in the *Hi3521 H.264 Codec Processor Data Sheet*.

Note the following when designing the board of Hi3521:

- The core power pin DVDD10 connects to the 1.0 V digital power. The DC-DC chip with 5 A or larger power supply capability is recommended.
- The input/output (I/O) power pin DVDD33 connects to the 3.3 V digital power. The estimated maximum current of DVDD33 is 350 mA.
- The DDR power pin DVDD1518 connects to the 1.5 V (DDR3) or 1.8 V (DDR2) digital power. The maximum current of DVDD1518 (excluding the current of the DDR) is 450 mA. It is recommended that all interconnected DDRs share the same power supply.
- The power supplies 3.3 V, 1.5 V/1.8 V, and 1.0 V must be powered on or power off in sequence, as shown in [Figure 1-4](#) and [Figure 1-5](#).

Figure 1-4 Power-on sequence

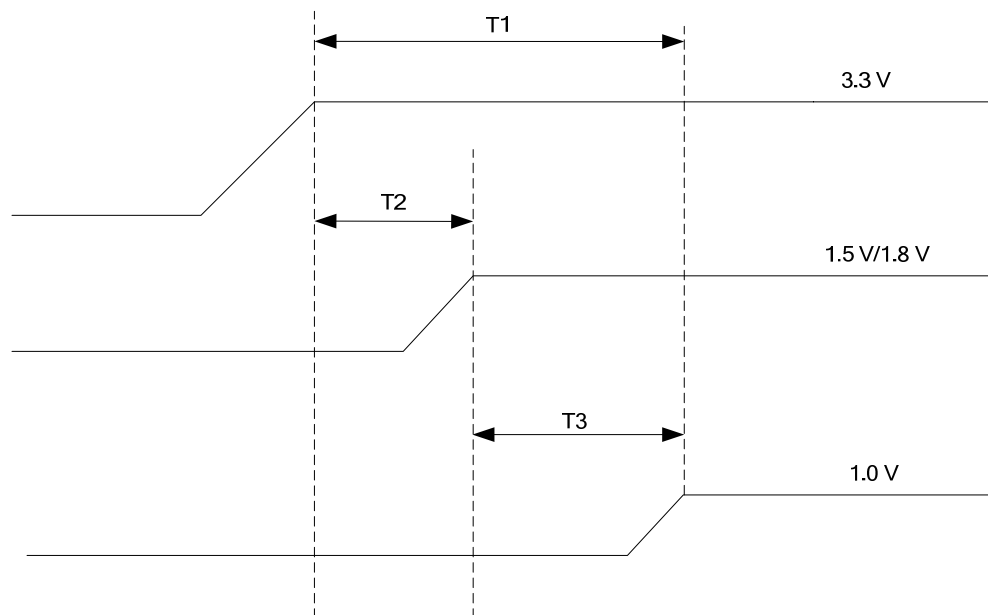
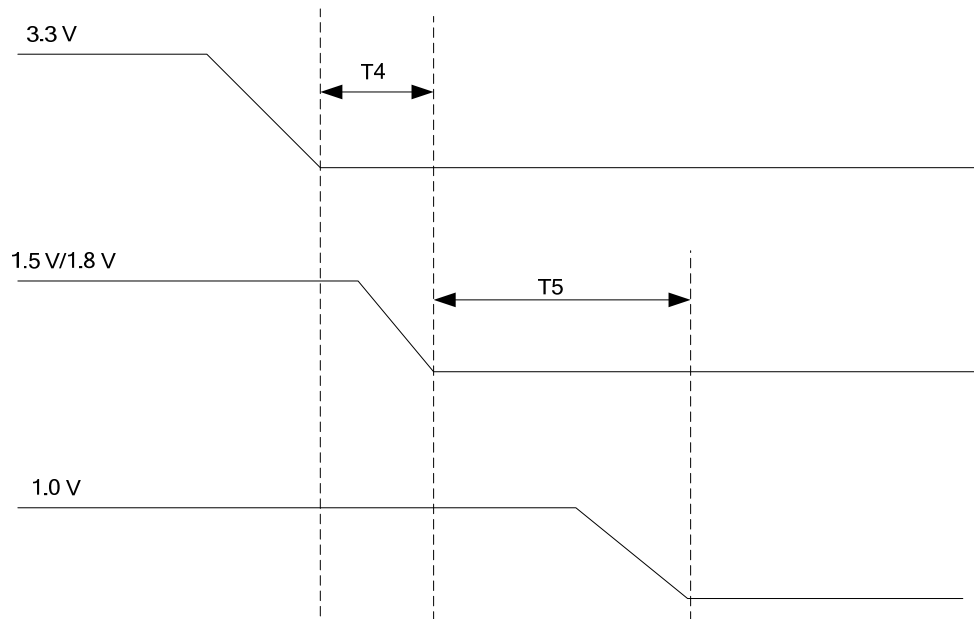




Figure 1-5 Power-off sequence



NOTE

$0 < T1 \leq 100 \text{ ms}$, $T2 > 0$, $T3 > 0$, $T4 > 0$, $T5 > 0$

- The phase-locked loop (PLL) power pins VDD10_PLL1, VDD10_PLL2345, VDDREF10_PLL2345, AVDD33_PLL1, and AVDD33_PLL2345 are isolated from the power pins DVDD10 and DVDD33 of the Hi3521 by using 1000 Ω @100 MHz ferrite beads. For details about circuits, see the schematic diagram of the Hi3521 demo board.
- Ensure that the output voltage of power supplies meets the requirements of the Hi3521 when the ripple and noise occur. For details about the requirements on the power supply of each module, see the "Electrical Specifications" section in the *Hi3521 Codec Processor Data Sheet*.

1.2 Design of Typical Interface Circuits

1.2.1 DDR2 and DDR3 Interfaces

1.2.1.1 Introduction

The Hi3521 DDR interface can be DDR2 interface complying with the stub series terminated logic for the 1.8 V (SSTL-18) standard or DDR3 interface complying with the SSTL-15 standard.

The Hi3521 double-data rate controller (DDRC) has the following features:

- Provides one DDRC interface. The DDRC has one DDRn synchronous dynamic random access memory (SDRAM) chip select (CS) and supports 32-bit or 16-bit data bus and configurable 15-bit address bus.



- Supports two mainstream 16-bit DDR2s with the maximum capacity of 256 MB (1 Gbit x 2 = 2 Gbits) or four mainstream 8-bit DDR2 with the maximum capacity of 512 MB (1 Gbit x 4 = 4 Gbits). The bus frequency ranges from 400 MHz to 533 MHz.
- Supports two mainstream 16-bit DDR3s with the maximum capacity of 1 GB (4 Gbit x 2 = 8 Gbits) or four mainstream 8-bit DDR3s with the maximum capacity of 1 GB (2 Gbits x 4 = 8 Gbits). The bus frequency ranges from 533 MHz to 620 MHz.
- Supports various low-power modes for the DDRn SDRAM including power down and self refresh modes.
- Supports the DDR3L.

1.2.1.2 Circuit Design Recommendations

DDR Topology

Figure 1-6 shows the typical external topology of connecting the external DDR3 SDRAMs, and Figure 1-7 shows the typical external DDR2 SDRAMs topology of the Hi3521.

Figure 1-6 Typical topology of connecting the Hi3521 to the external DDR3 SDRAMs (taking one DDRC interface as an example)

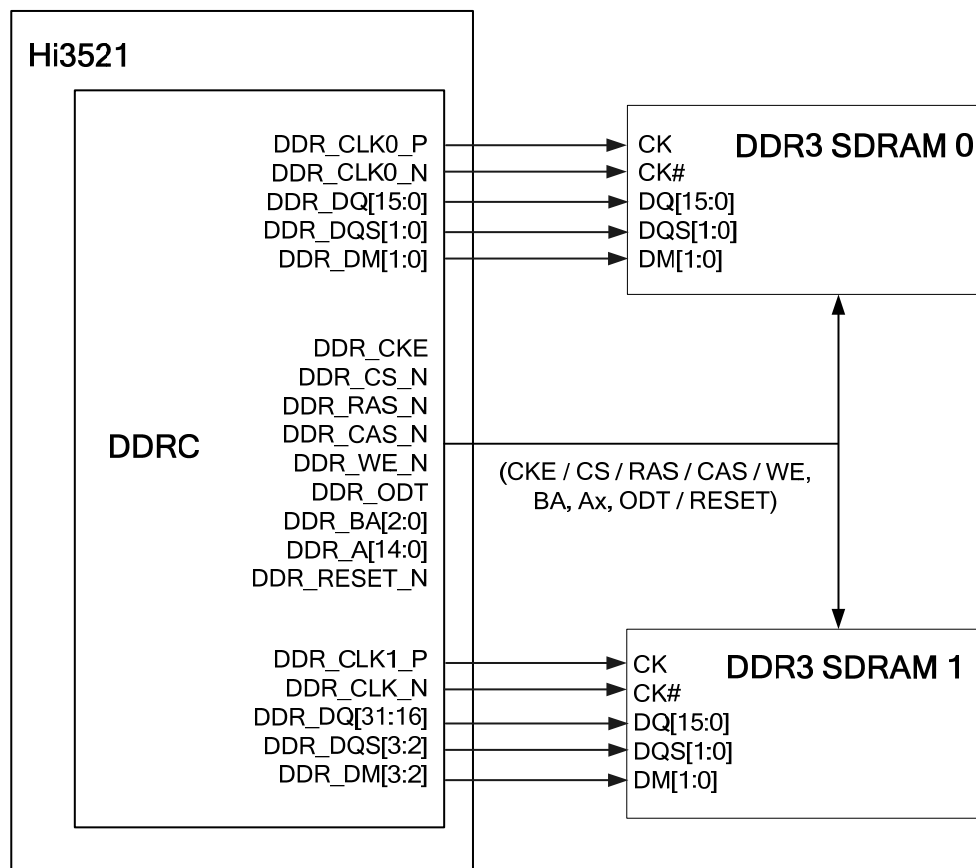
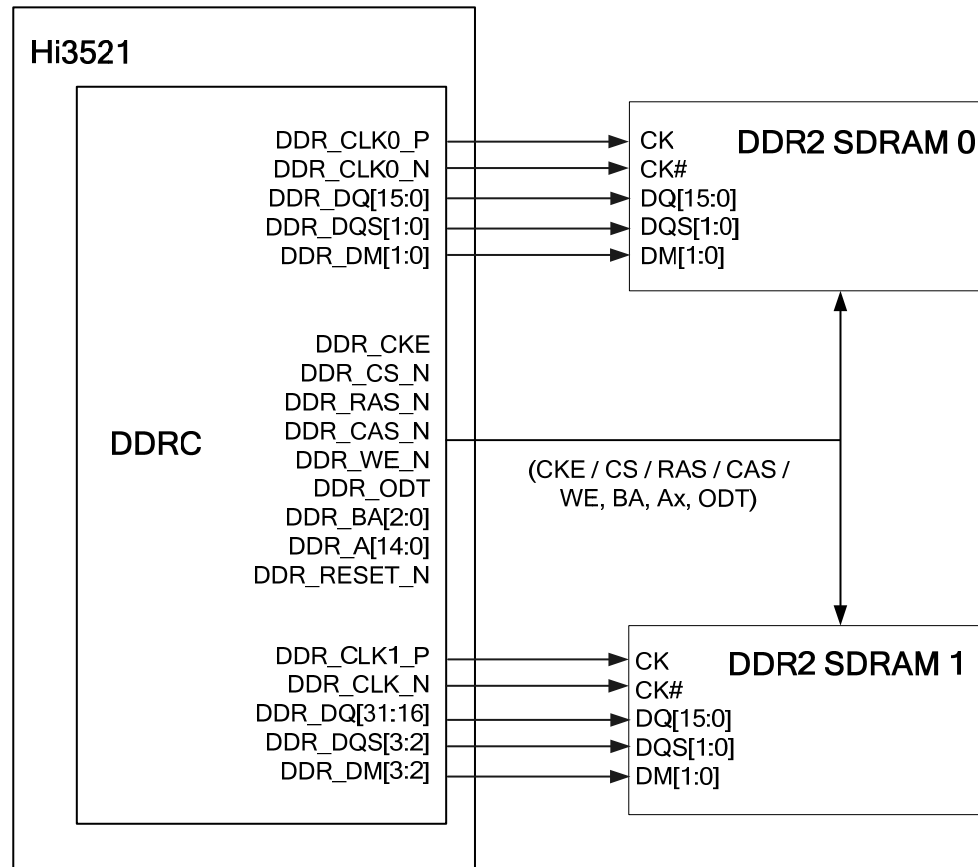


Figure 1-7 Typical topology of connecting the Hi3521 to the external DDR2 SDRAMs



Design of the DDR Power Supply

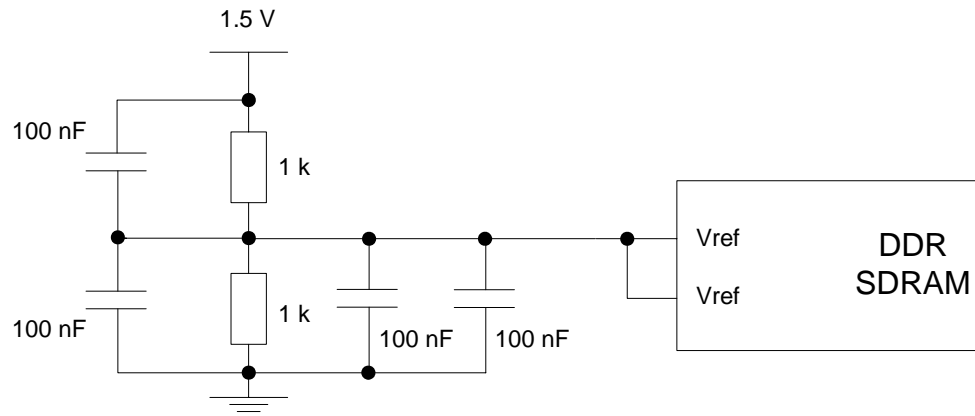
The Hi3521 DDRC and interfaces comply with the DDR3 SSTL-15 and SSTL-18 standards. The 1.5 V or 1.8 V power supplies and 0.75 V or 0.9 V reference voltages V_{ref} are required. The 1.5 V or 1.8 V power supplies of the Hi3521 and the DDRs must be unified.

It is recommended that you design a separate direct current (DC) to DC circuit on the board to supply power for the DDR2 or DDR3 and the 1.5 V or 1.8 V power pins of the Hi3521 DDRC. You must supply 0.75 V or 0.9 V reference voltages for the DDR2 or DDR3 and the reference power pin V_{ref} of the Hi3521 DDRC by using 1% voltage-divider resistors. In addition, you must connect a 0.1 μ F decoupling capacitor close to each power pin and reference power pin.

Figure 1-8 shows the reference design of the DDR3 voltage-divider circuit. The DDR2 voltage-divider circuit is similar to the circuit shown in Figure 1-8, but the voltage changes to 1.8 V.



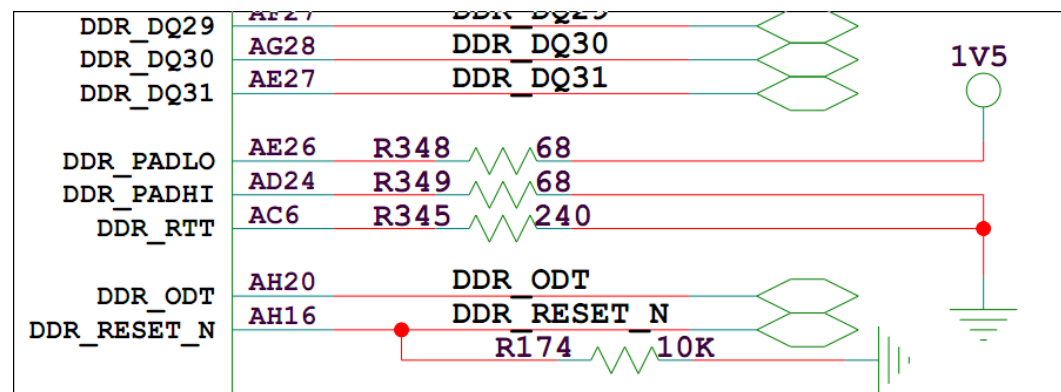
Figure 1-8 Reference design of the DDR3 voltage-divider circuit



Design of the DDR_PADLO, DDR_PADHI, and DDR_RTT Pins

DDR_PADLO and DDR_PADHI are used for drive compensation. A pull-down resistor must be connected between DDR_PADHI and GND, and a pull-up resistor must be connected between DDR_PADLO and common connector voltage (VCC). These resistors determine the drive impedance of DDRC pins. See [Figure 1-9](#).

Figure 1-9 Connection mode of the DDR_PADLO, DDR_PADHI, and DDR_RTT pins



- For the DDR2, the SSTL_1.8V_ClassI mode is selected. In this mode, a 68 Ω pull-up resistor is used, and the drive impedance is 34 Ω. See [Table 1-4](#).
- For the DDR3, the SSTL_1.5V mode is selected. In this mode, a 68 Ω pull-up resistor is used, and the drive impedance is 34 Ω. See [Table 1-4](#).

Table 1-4 Relationships between the pull-up and pull-down resistors of DDR_PADLO and DDR_PADHI pins and the drive impedance of DDRC pins

Mode	Pull-Up Resistor (Ω)	Pull-Down Resistor (Ω)	Drive Impedance (Ω)
HSTL_1.5V_ClassI	78	78	39



Mode	Pull-Up Resistor (Ω)	Pull-Down Resistor (Ω)	Drive Impedance (Ω)
HSTL_1.5V_ClassII	44	44	22
SSTL_1.8V_ClassI	68	68	34
SSTL_1.8V_ClassII	38	38	19
SSTL_2.5V_ClassI	78	78	39
SSTL_2.5V_ClassII	43	43	21.5
SSTL_1.5V	68	68	34

The DDR_RTT pin is used for RTT compensation. A resistor must be connected between DDR_RTT and GND. This resistor and the configurations of internal registers determine the on-die termination (ODT) impedance.

A 300 Ω external resistor is typically used for the DDR2. As shown in [Table 1-5](#), if the value of the REN75 register is 0 and the value of the REN150 register is 1, the ODT impedance is 150 Ω ; if the value of REN75 is 1 and the value of REN150 is X, the ODT impedance is 75 Ω .

A 240 Ω external resistor is typically used for the DDR3. As shown in [Table 1-5](#), if the value of REN75 is 0 and the value of REN150 is 1, the ODT impedance is 120 Ω ; if the value of REN75 is 1, and the value of REN150 is X, the ODT impedance is 60 Ω .

Table 1-5 ODT impedance

REN75	REN150	External Resistance	RTT Value
0	0	Any	No RTT
0	1	200	100
0	1	240	120
0	1	300	150
1	X	200	50
1	X	240	60
1	X	300	75

1.2.1.3 Design Recommendations for Matched Modes

Bidirectional Signals DQ and DQS

In the Hi3521 DDR application, the point-to-point topology is used for the data input/output (DQ), DQS_P, and DQS_N signals. The details are as follows:

- When DDR2s are connected:

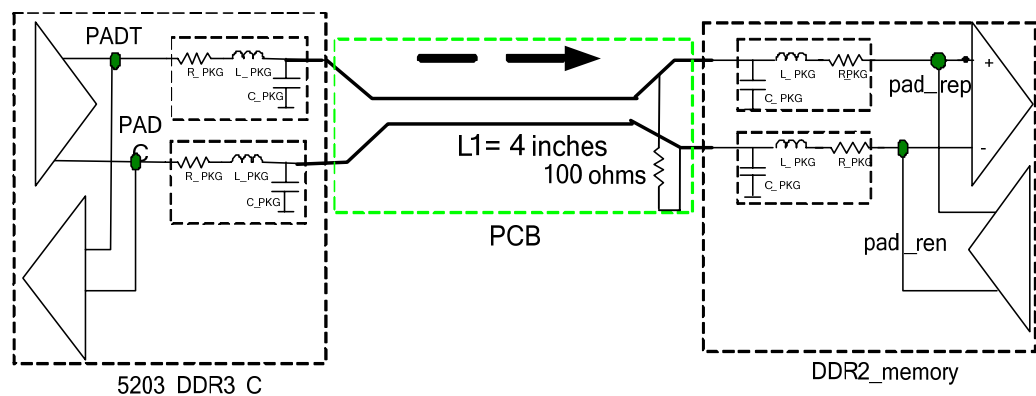
- When data is written (that is the data is output from the Hi3521), the DDR2s connect to the Hi3521 directly, the SSTL_1.8V_ClassI mode is used, and the ODT resistor is set to 75 Ω at the DDR2 end.
- When data is read (that is the data is input to the Hi3521), the DDR2s connect to the Hi3521 directly and the ODT resistor is set to 75 Ω at the Hi3521 end.
- When DDR3s are connected:
 - When data is written (that is the data is output from the Hi3521) the DDR3s connect to the Hi3521 directly. The output impedance on the Hi3521 side is 34 Ω and the ODT resistor is set to 60 Ω at the DDR end.
 - When data is read (that is the data is input to the Hi3521), the DDR3s connect to the Hi3521 directly. The output impedance on the DDR3 side is 34 Ω and the ODT resistor is set to 60 Ω at the Hi3521 end.

Differential Clock

In the Hi3521 DDR application, the differential signals DDR_CLK_N and DDR_CLK_P support the following one-drive-one and one-drive-two modes:

- When DDR2s are connected:
 - In single-load mode, when data is written and a 100 Ω resistor connects to the DDR, as shown in [Figure 1-10](#).

Figure 1-10 Differential clocks DDR_CLK_N and DDR_CLK_P in one-drive-one mode in the DDR2 application

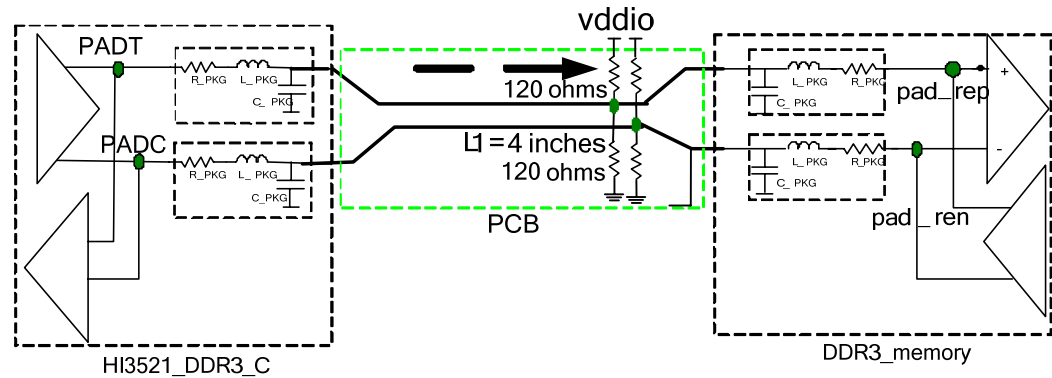


NOTE

The trace length in [Figure 1-10](#) is the maximum value, the actual trace length is less than the maximum value. This rule is applicable to the trace length in [Figure 1-11](#).

- When DDR3s are connected:
 - In single-load mode, the clock signals DDR_CLK_N and DDR_CLK_P at the load end are pulled up to the 1.5 V power supply respectively over 120 Ω resistors and pulled down to GND respectively over 120 Ω resistors, as shown in [Figure 1-11](#).

Figure 1-11 Differential clocks DDR_CLK_N and DDR_CLK_P in one-drive-one mode in the DDR3 application



Address Signal and Control Signal

The address and control signals of the DDR2 or DDR3 support the following two modes: one-drive-one mode and one-drive-two mode (The following example is based on the data width of 16 bits).

When DDR2s are connected:

- In single-load mode, the DDR2 connects to the Hi3521 directly, as shown in [Figure 1-12](#).
- In dual-load mode, the DDR2 connects to the Hi3521 directly and the T-shaped topology is used, as shown in [Figure 1-13](#).

Figure 1-12 Address signal and control signal in one-drive-one mode

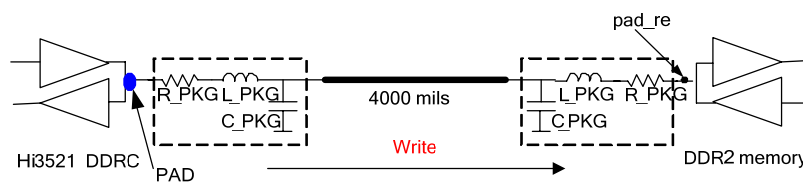
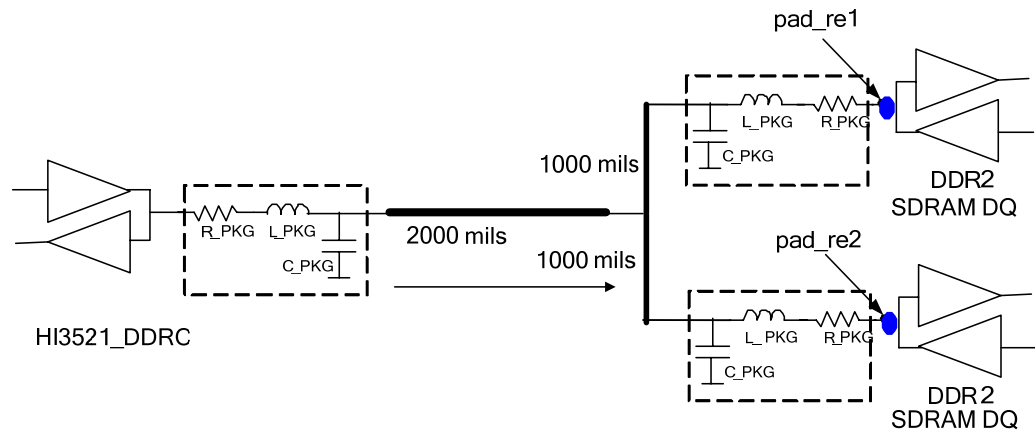


Figure 1-13 Address signal and control signal in one-drive-two mode



When DDR3s are connected:

- In single-load mode, the DDR3 connects to the Hi3521 directly, as shown in [b](#).
- In dual-load mode, the T-shaped topology is used, as shown in [Figure 1-13](#). In addition, two 22 Ω resistors are connected in series between the T point and DDRs, as shown in [Figure 1-16](#).

Figure 1-14 Address signal and control signal in single-load mode

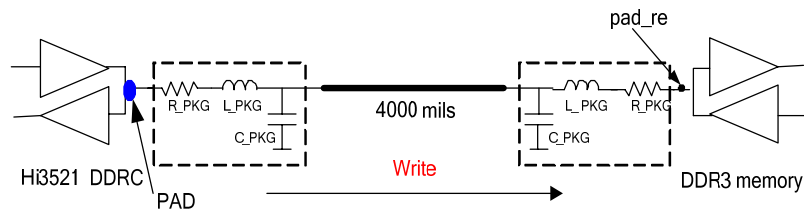


Figure 1-15 Address signal and control signal in dual-load mode

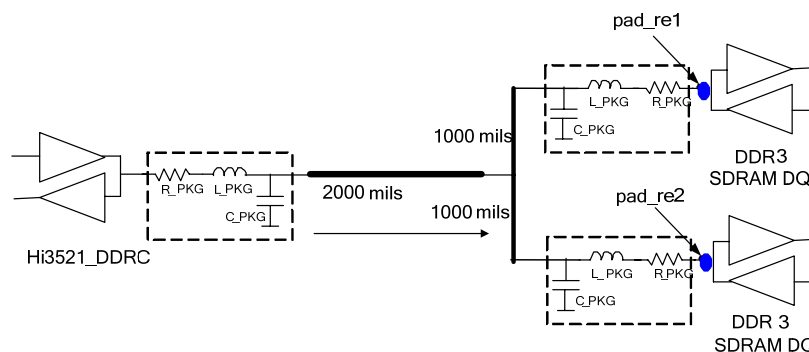
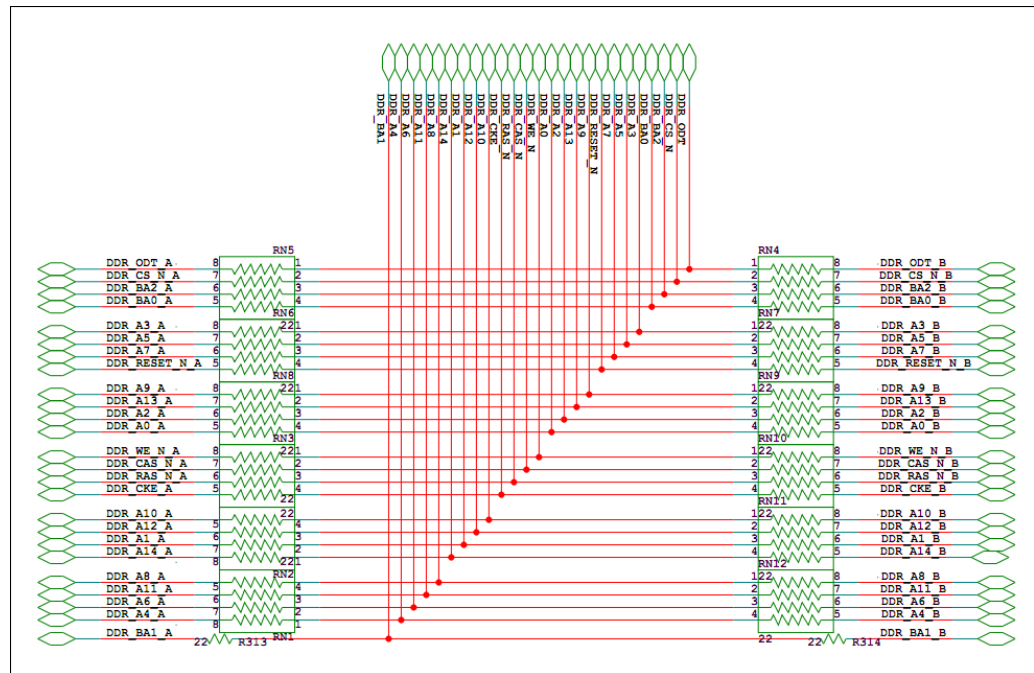




Figure 1-16 Resistors in series between the T point and DDRs



DM Signal

In the Hi3521 DDR3 or DDR2 application, the point-to-point topology is used, and the data mask (DM) signal is connected directly.

1.2.1.4 Recommendations for Component Selection

The DDR3 supports the maximum working frequency of 620 MHz and the DDR2 supports the maximum working frequency of 533 MHz. The current mainstream DDR3s and DDR2s meet the requirements and DDRs are selected based on the capacity requirements and cost.

1.2.2 USB 2.0 Host Port

1.2.2.1 Introduction

The Hi3521 USB 2.0 host port complies with the USB 2.0 protocol and supports low-speed, high-speed, and full-speed modes. As the USB 2.0 host module is independent, you can disable it when no data is transferred. This reduces the power consumption of the Hi3521.

1.2.2.2 Design Recommendations for the USB Circuit

Design Recommendations for the USB Power

The analog power AVDD33_USB must be isolated from the digital power. You are advised to use planes to reduce the parasitic effect, decoupling noise, and power supply impedance. In addition, filtering capacitors are required and must be placed close to pins.

The digital power DVDD10_USB and digital GND DVSS_USB must be not interfered, and short and wide traces are used.



Design Recommendations for the USB Protective Circuit

A protective circuit must be designed in the USB circuit for meeting the requirements for the electrostatic discharge (ESD) protection. To avoid the USB routing signals from being affected by protective components, design the PCB according to the following guidelines:

- Place the protective components close to the USB connector port.
- Ensure that the parasitic capacitors of the protective components connected to the high-speed USB 2.0 port are less than 1 pF, and the response time is less than 1 ns.

1.2.3 GMAC Port

The Hi3521 gigabit media access controller (GMAC) port supports the reduced gigabit media independent interface (RGMII) mode and media independent interface (MII) mode. You must pay attention to the connection modes of the TXCKOUT and TXCK pins. In RGMII mode, the RGMII_TXCKOUT of the Hi3521 connects to the GTXCLK pin of the PHY, as shown in [Figure 1-17](#). In MII mode, the RGMII_TXCK pin of the Hi3521 connects to the TXCLK pin of the PHY, as shown in [Figure 1-18](#).

Figure 1-17 Signal connection in RGMII mode

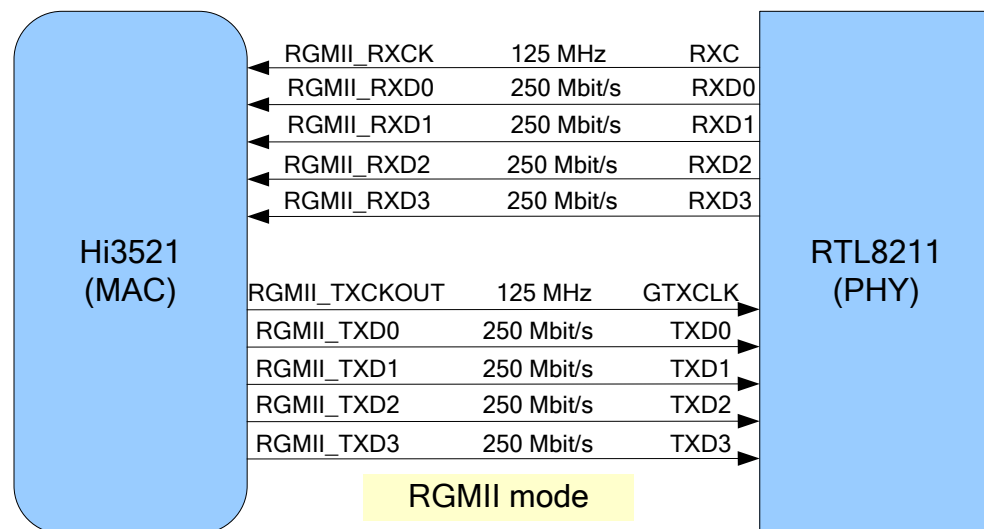
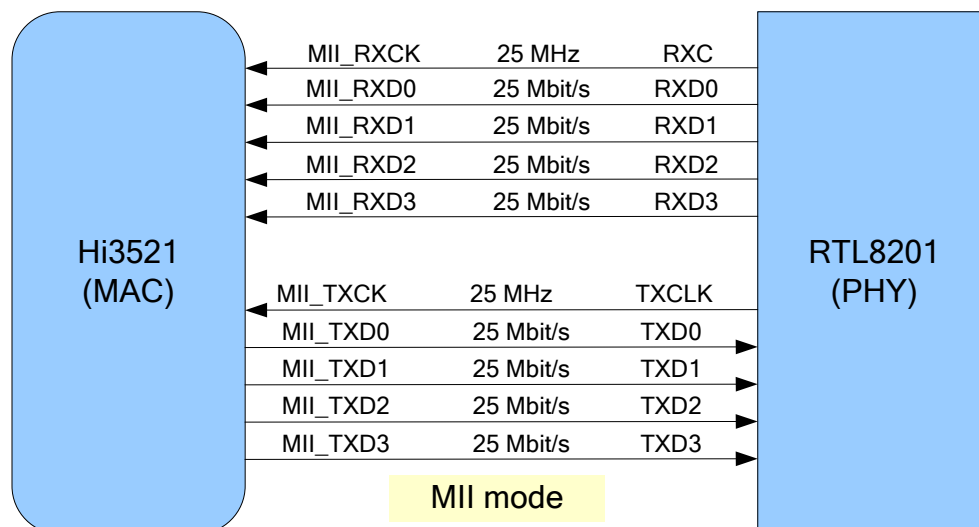




Figure 1-18 Signal connection in MII mode



All the signals of the GMAC port are connected by using the point-to-point topology. Therefore, each PCB trace must be less than or equal to 6 inches. The design recommendations for matched resistors are as follows:

- Connect a 4.7 k Ω pull-up resistor to the MDIO signal.
- Connect 22 Ω resistors in series to the signals TXD0 to TXD3 close to the Hi3521.
- Connect a 33 Ω resistor in series to the TXCLK signal close to the PHY in MII mode.
- Connect a 22 Ω resistor in series to the GTXCLK signal close to the Hi3521.
- Connect 22 Ω resistors in series to the signals RXD0 to RXD3 close to the PHY.
- Connect a 22 Ω resistor in series to the RGMII_RXCK signal close to the PHY.

1.2.4 Flash Interface

The Hi3521 supports the NAND flash and SPI NOR flash. You can determine the topology and matched mode based on the actual load scheme and board conditions.

The Hi3521 NAND flash controller (NFC) and SPI NOR flash controller (SFC) each have two CSs. With the CSs, the Hi3521 can be connected to the component with two CS pins and be applicable in the application with two flash memories.



CAUTION

- If the Hi3521 boots from the SPI NOR flash, the CS of SPI NOR flash must be connected to SFC_CS1N of the Hi3521.
- If the Hi3521 boots from the NAND flash, the CS of the NAND flash must be connected to NF_CSN0 of the Hi3521.



1.2.5 Design Recommendations for the SATA Interfaces

The Hi3521 provides two SATA 2.6 interfaces. Each SATA interface supports the PM function, eSATA function, and clock gating. When the SATA interfaces are not in use, they can be switched to the power-down mode to reduce the power consumption. Note the following:

- The 1.0 V and 2.5 V power supplies for the SATA interfaces must be isolated from the 1.0 V and 2.5 V power supplies for the system. Filtering capacitors are placed close to the pins.
- 10 nF capacitor on the Rx and Tx signals of the SATA interface must be close to the SATA socket.
- If the 15 V and 5 V power supplies are provided for the SATA interface through the main board. Filtering is recommended for the two power supplies.
- The trace length is less than or equal to 5 inches.

1.2.6 Design Recommendations for the SPI Control Interface

The Hi3521 provides one SPI clock signal pin, one data input pin, one data output pin, and four CS signals, which are used to connect the peripherals with SPI interfaces. The maximum frequency of SPI_CLK is 40 MHz. Note the following:

- In single-load mode, you are advised to connect a 47 Ω resistor in series to the source end and connect a 33 Ω resistor in series to each source end of two data lines.
- In multi-load mode, the daisy chain connection is recommended for SPI_CLK. The trace delay and the delay of passing through the components must be considered when you configure the working frequency of SPI_CLK. The reference delay of the 1000-mil trace is 180 ps.

1.2.7 Design Recommendations for the I²S Interface

The Hi3521 provides the following three sets of I²S audio signal interfaces: SIO0, SIO1, and SIO2. Note the following:

- SIO0 and SIO1 act only as input interfaces.
- SIO2 acts as I/O interfaces.

1.2.8 Design Recommendations for the HDMI Output Interface

The Hi3521 has an embedded high-definition multimedia interface (HDMI) PHY that outputs the HDMI signals directly.

- The 1.0 V power supplied to the HDMI interface must be isolated from the 1.0 V power of the system by using ferrite beads, and sufficient filtering capacitors are connected close to pins. The 1000 Ω @100 MHz ferrite beads are recommended. The 100 nF/6.3 V ceramic capacitors must be connected after the ferrite beads.
- The HDMI_REXT pin connects to the external reference resistor and you are advised to use a 1% 6.8 k Ω resistor and a 51 k Ω resistor in parallel.
- The four sets of HDMI difference signals require ESD protection, the ESD components must be placed close to the HDMI interface.
- The dedicated I²C signal for the HDMI interface can connect to the HDMI interface only after its level is changed from 3.3 V to 5 V.
- Reverse flow prevention design is recommended for the HDMI interface circuit. For details, see the schematic diagram of the Hi3521 demo board.



1.2.9 Design Recommendations for the Analog DAC Interface

The Hi3521 provides two sets of video DACs.

- The VDAC0_IOUT0 and VDAC0_IOUT1 pins of the first set video DAC act as the outputs of the composite video broadcast signal (CVBS) signals. The impedance must be matched. Note that the VDAC0_IOUT2 pin does not output analog signals, it must be connected to GND over an external 75 Ω resistor. VDAC0_VDREF must be connected to GND over 10 nF and 1 nF capacitors in parallel. VDAC0_IREF must be connected to GND over 1% 1.1 k Ω and 51 k Ω external resistors in parallel. For details, see the schematic diagram of the Hi3521 demo board.
- The VDAC1_IOUT0, VDAC1_IOUT1, and VDAC1_IOUT2 pins of the second set video DAC are used to output the Pr/B, Pb/G, and Y/R signals respectively. The impedance must be matched. VDAC1_VDREF must be connected to GND over 10 nF and 1 nF resistors in parallel. VDAC1_IREF must be connected to GND over 1% 1.1 k Ω and 51 k Ω internal resistors in parallel. The R, G, B signals and the VGA_HS/VGA_VS are output as VGA signals. For details, see the schematic diagram of the Hi3521 demo board.
- The 3.3 V power supplies of the two sets of video DACs must be isolated from the 3.3 V power of the system and sufficient filtering capacitors are placed close to the 3.3 V power pin of the analog DAC.
- Note that the high-definition (HD) picture-in-picture (PIP) function is multiplexed with the CVBS0 output function. If the PIP function is used, the CVBS0 output is unavailable. That is, if the HD PIP and standard-definition (SD) CVBS output functions are required at the same time, the SD CVBS signals must be output from the CVBS1 interface.

1.2.10 Design Recommendations for VI and VO Interfaces

The Hi3521 has three BT.1120 physical interfaces and a BT.656 interface. Their features are as follows:

- VIU0 and VIU1 act as BT.1120 input interfaces.
- The VOU1120 interface acts as the BT.1120 output interface, and the VOU656 interface acts as the BT.656 output interface.
- VOU1120 works with VOU656 to act as the 24-bit RGB signal output interface for the LCD.
- The VIU0 and VIU1 interfaces can be divided into two BT.656 input interfaces respectively. In this case, the VIUx_CLK signal can act as the upper eight-bit sampling clock signal and the VIUx_VS signal can act as the lower eight-bit sampling clock signal. The encoding performance of the upper eight bits is the same as that of the lower eight bits.
- VOU656 is multiplexed as the SD card interface.

Table 1-6 describes the multiplexing relationships between the VOU1120 and VOU656 signals. For details, see the description of the pins of the Hi3521. For details about the circuit design, see the schematic diagram of the Hi3521 demo board.

Table 1-6 Multiplexing relationships between the VOU1120 and VOU656 signals

Signal	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
VOU1120	VOU1120	LCD_B, LCD_G	None



VOU656	VOU656	LCD_R	SDIO
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2 PCB Design Recommendations

2.1 Design Recommendations for the Fanout Package

The body size of the Hi3521 is 19 mm x 19 mm (0.75 in. x 0.75 in.). It has 449 pins, and its ball pitch is 0.8 mm (0.031 in.) in the core power area or 0.65 mm (0.026 in.) in other areas. For details about the body size and the package of the Hi3521, see chapter 2 "Hardware" in the *Hi3521 H.264 Codec Processor Data Sheet*.

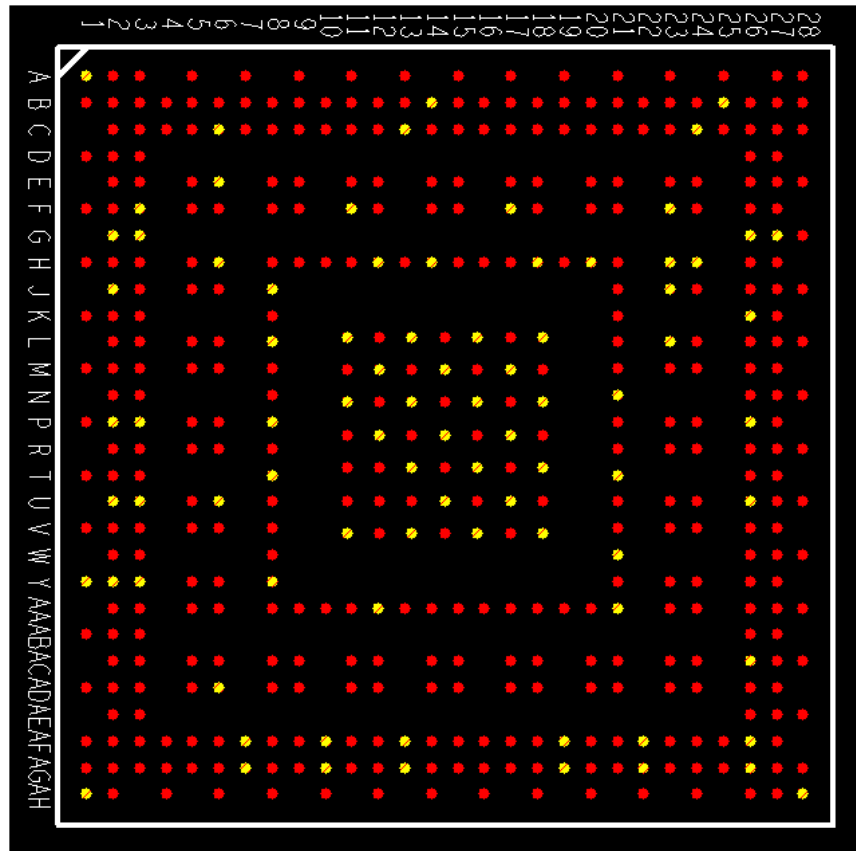
To ensure signal integrity and reduce the cost, you are advised to use a 4-layer PCB with the following stack when routing all Hi3521 signal traces:

- Top layer: signal 1 (component layer 1)
- Layer 2: GND layer
- Layer 3: power layer
- Bottom layer: signal 4 (component layer 2)

[Figure 2-1](#) shows the pinout.



Figure 2-1 Pinout



The pins in the six outer circles are power pins and GND pins of some modules and signal pins. The pins in the middle are the core power pins and GND pins. [Figure 2-2](#) shows the arrangement of the pins in the middle.



Figure 2-2 Arrangement of the powers and the GND pins in the middle

VSS	VDD	VSS	VDD	VSS	VDD	VSS
VDD	VSS	VDD	VSS	VDD	VSS	VDD
VSS	VDD	VSS	VDD	VSS	VDD	VSS
VDD	VSS	VDD	VSS	VDD	VSS	VDD
VSS	VDD	VSS	VDD	VSS	VDD	VSS
VDD	VSS	VDD	VSS	VDD	VSS	VDD
VSS	VDD	VSS	VDD	VSS	VDD	VSS

Note the following during the fanout design: As the body size of the Hi3521 is 19 mm x 19 mm (0.75 in. x 0.75 in.), pay attention to the fanout mode of the pins in the outer six circles and via position, ensuring the overcurrent performance of the power layer and smooth current return paths of the GND layer. To be specific, the traces of the pins in the outmost three circles are fanned out from the top layer, see [Figure 2-3](#). The vias around the pins in other three circles must be punched in a specific pattern. This ensures the integrity of the GND layer and power layer. [Figure 2-4](#) shows the recommended vias at the GND layer, and [Figure 2-5](#) shows the recommended vias at the power layer.



Figure 2-3 Vias between pins (blue dots)

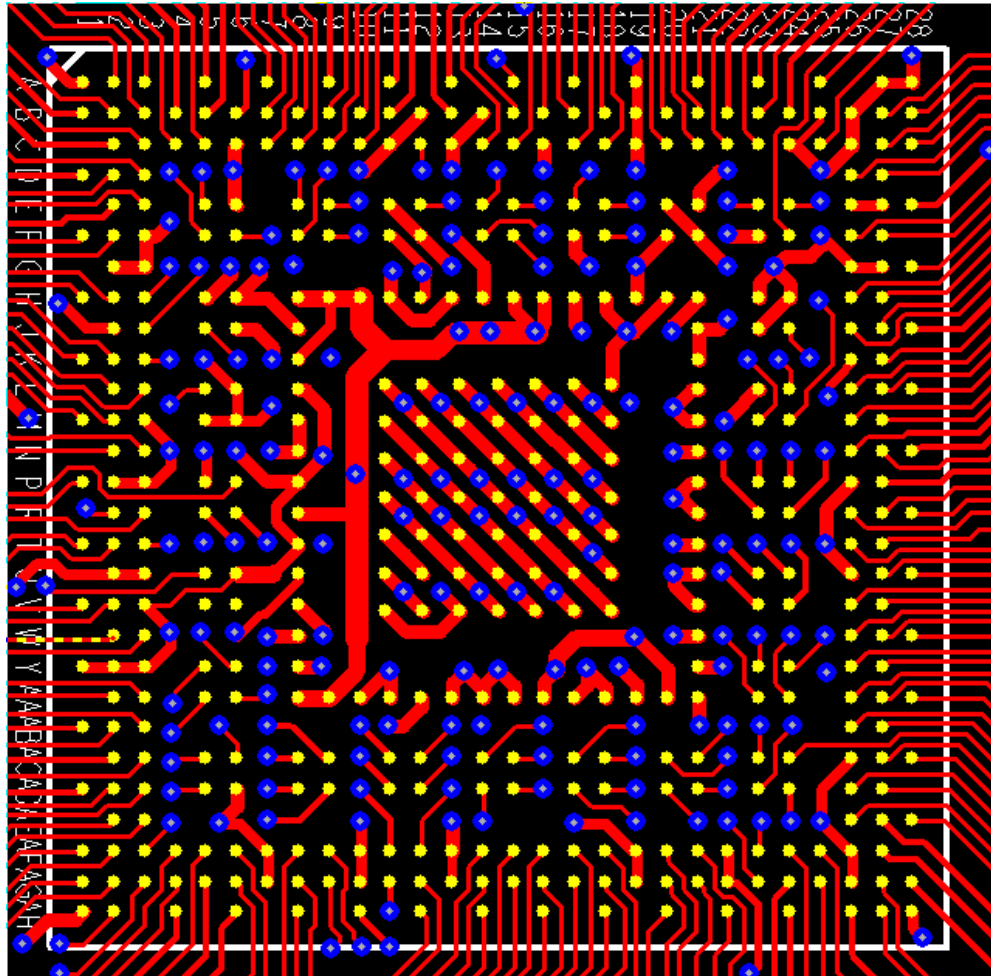




Figure 2-4 Current return paths under the Hi3521 at the GND layer when vias are punched between pins

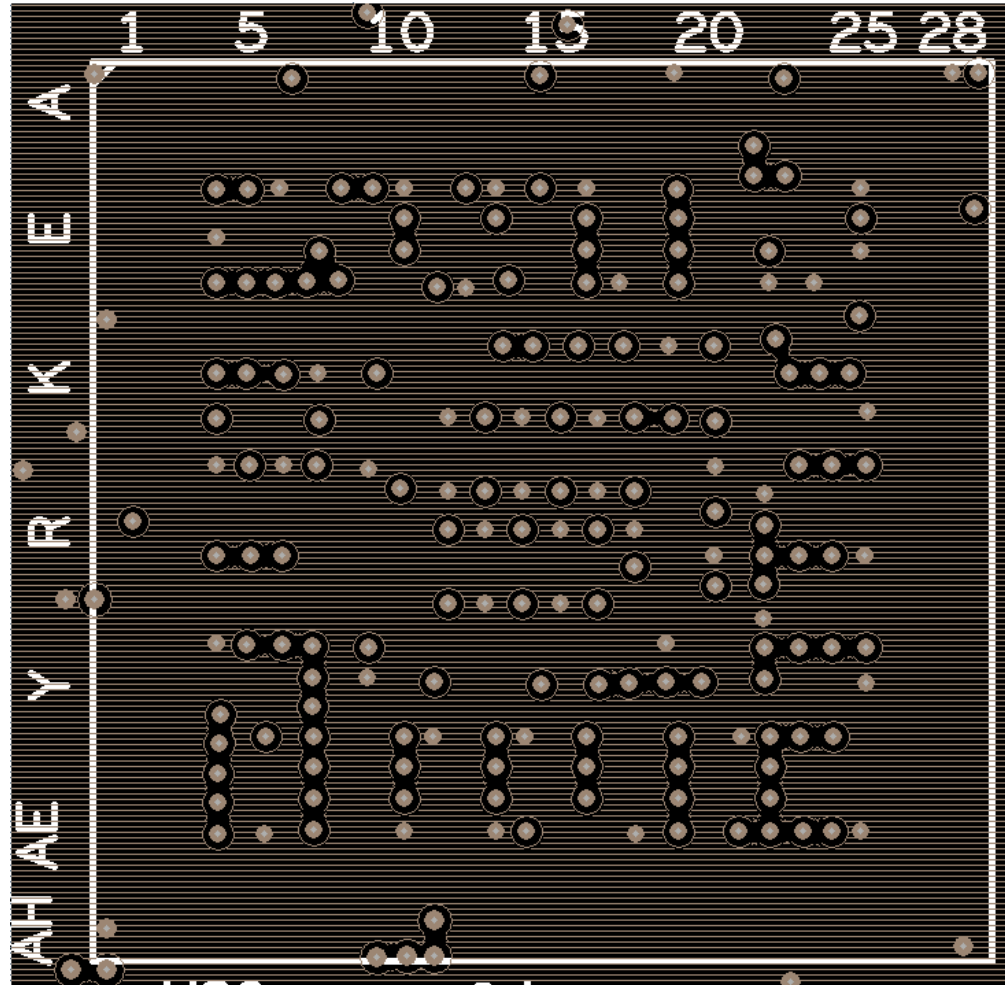
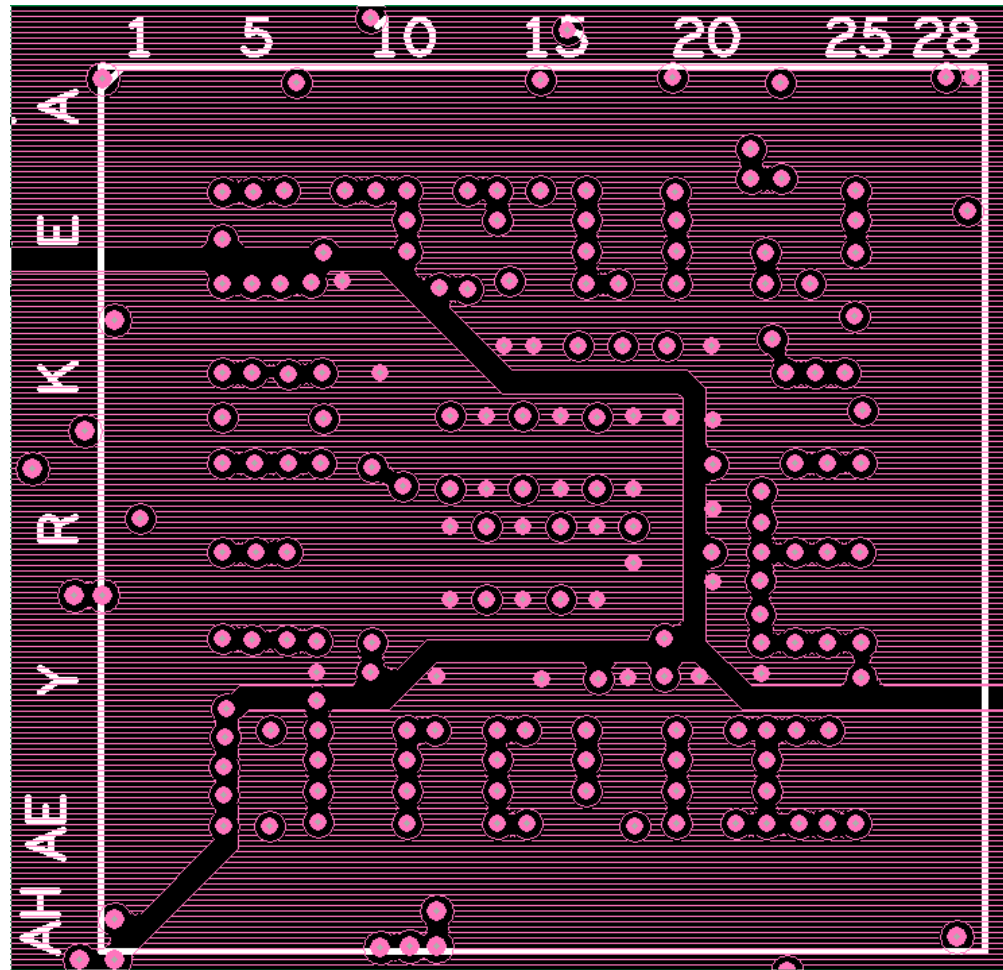


Figure 2-5 Current return paths under the Hi3521 at the power layer when vias are punched between pins

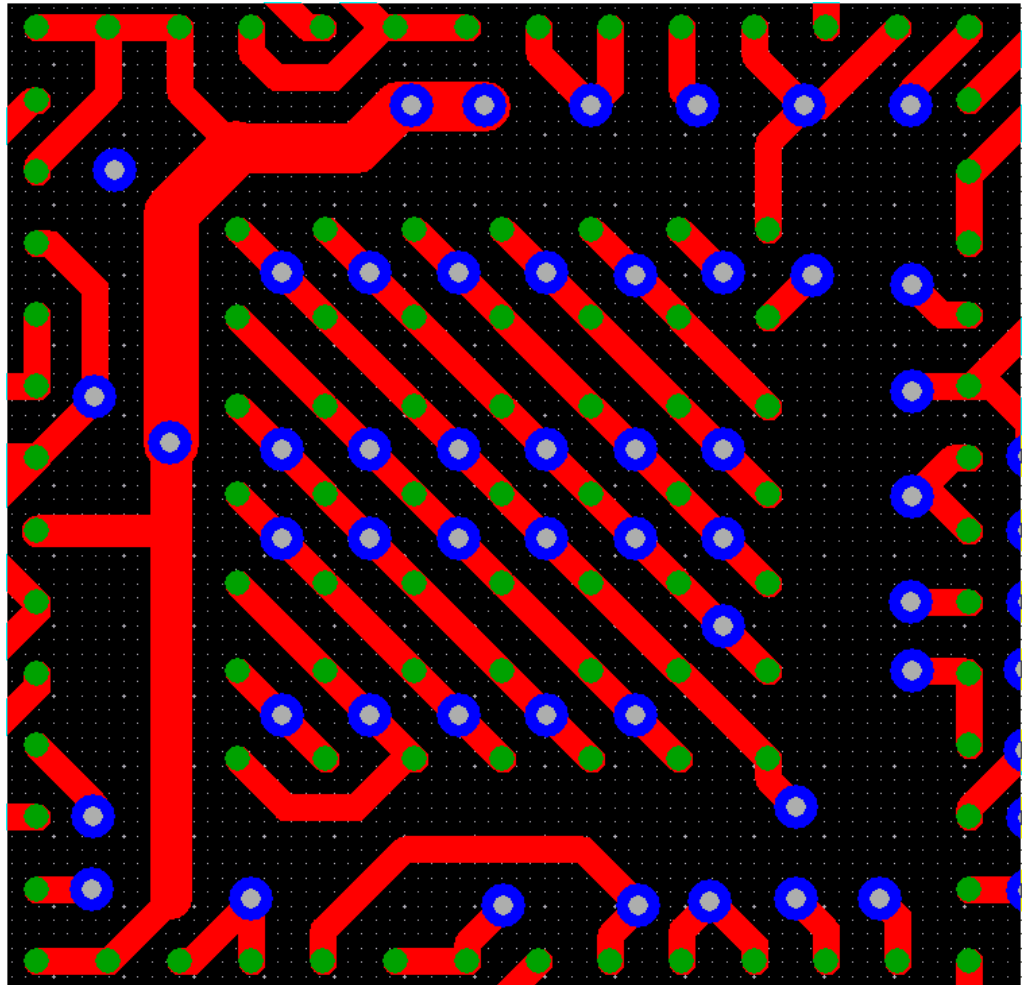


Ensure that the power supplies for the 3.3 V, 1.5 V, and 1.0 V power pins are provided through complete power planes. In addition, the copper plane for the 1.0 V core power must be wide to support 5 A overcurrent performance.

2.2 Design Recommendations for the Core Power Area

2.2.1 Core Power Routing and Vias

To ensure the overcurrent performance of the core power, you are advised to route the traces between the soldering pads on the top surface in the way shown in [Figure 2-6](#). Note that at most two soldering pads share a via. If the via diameter is 8 mils and the soldering pad diameter is 16 mils, more than 14 such vias are required.

Figure 2-6 Top surface of the core power area

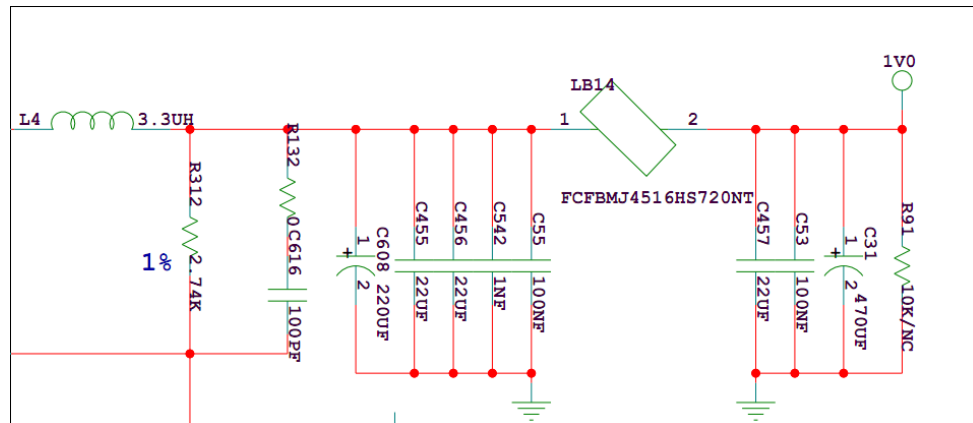
2.2.2 Core Power and Filtering Capacitors

The following points are taken into account to ensure the core power quality:

π -Shaped Filtering at the Output End of DC-DC

The DC-DC solution that features rapid transient response and high conversion efficiency while light loading is recommended. At the DC-DC output end, you are advised to place electrolytic capacitors after FERRITE beads to form a π -shaped filtering circuit. [Figure 2-7](#) shows the 1.0 V filtering circuit.

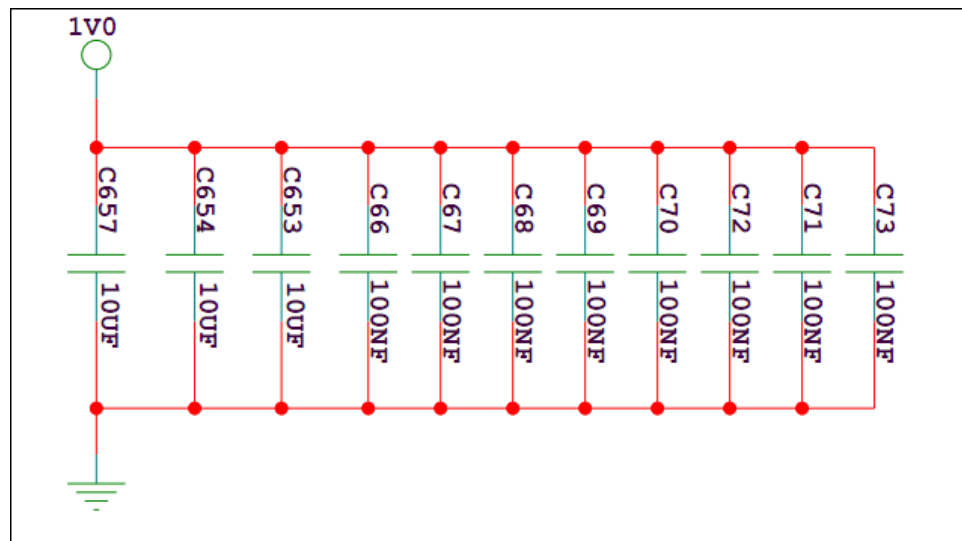
Figure 2-7 1.0 V filtering circuit



Capacitor Quantity

There are high requirements on the number of capacitors for the 1V0_Core power. The core power has 24 pins. At most two pins share a via, one 100 nF filtering capacitor must be placed close to each via, and three 10 μ F capacitors must be placed. See [Figure 2-8](#).

Figure 2-8 Filtering capacitors in the 1.0 V filtering circuit



Capacitor Layout

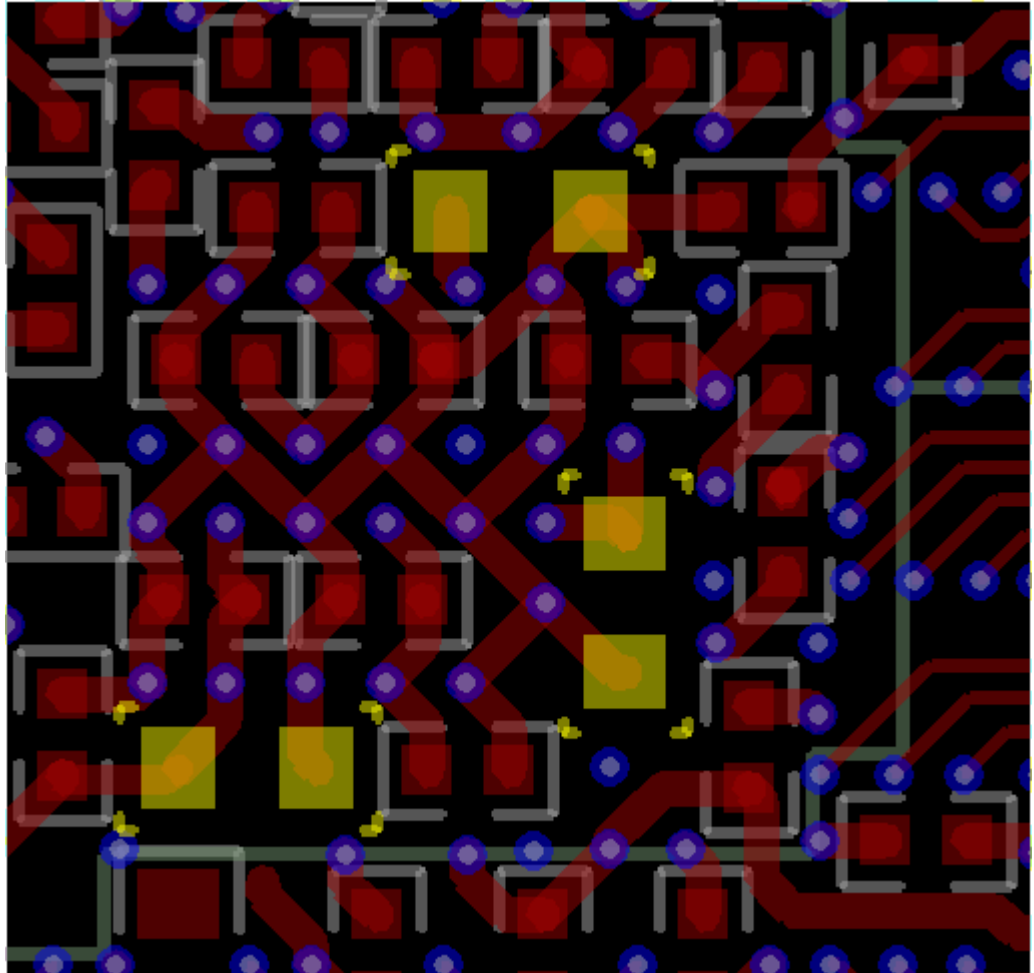
The capacitors for the 1V0_Core power must be placed in the area facing the bottom surface of the master chip. The details are as follows:

- A capacitor is placed close to each 1V0_Core power via under the bottom surface of the master chip, and the spacing between a capacitor and a via must less than 50 mils.
- The 10 μ F filtering capacitors must be placed in the middle of the core power area.

- One 100 μ F tantalum capacitor is recommended outside the area facing the bottom surface of the master chip.

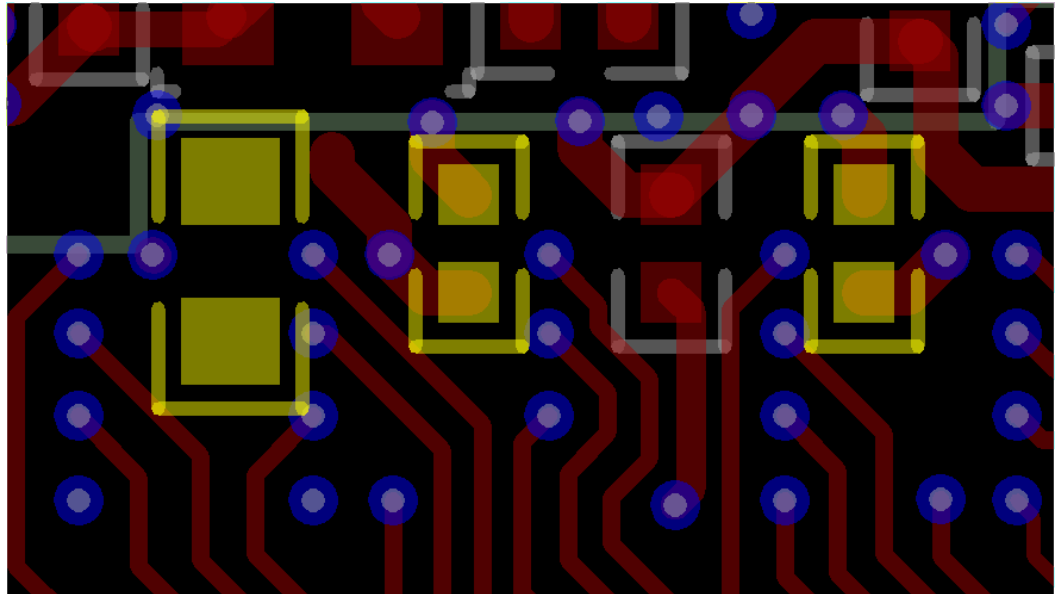
Figure 2-9 shows the capacitors for the 1V0_Core power that are placed in the area facing the bottom surface of the master chip.

Figure 2-9 Capacitors placed in the area facing the bottom surface of the master chip (for the 1V0_Core power)



The requirements on the 1.5 V power at the chip end are the same as those on the 1V0_Core power. To be specific, at most two soldering pads share a via, one 100 nF filtering capacitor is placed close to each via, and at least one 10 μ F ceramic capacitor is placed close to vias. See Figure 2-10.

Figure 2-10 Capacitors placed in the area facing the bottom face of the master chip (for the 1.5 V power)



2.3 DDR2 or DDR3 SDRAM Interface

2.3.1 Power Supply Design

To meet the requirement on the DDR2 and DDR3 bus bandwidth, the Hi3521 is integrated with a port drive supporting the SSTL-15 and SSTL-18 standards. Therefore, you are advised to route the board traces according to the SSTL-15 and SSTL-18 signal routing specifications.

The VREF power supplies (0.9 V for the DDR2 SDRAM and 0.75 V for the DDR3 SDRAM) and the power supplies of the Hi3521 must be isolated from other power supplies. You can connect the Hi3521 and the DDR2 or DDR3 SDRAM by using wide traces (15 mils or wider). Ensure that decoupling capacitors are placed close to each power pin and the VREF is masked by surrounding ground traces. The 1.5 V or 1.8 V power pins of the DDR2 or DDR3 and the Hi3521 DDR need to be connected on a same power network and decoupling capacitors need to be placed close to the power pins.

Connect four or more 10 μ F capacitors on the 1.5 V or 1.8 V power paths, as shown in [Figure 2-11](#) and [Figure 2-12](#). For details, see the Hi3521 demo board.



Figure 2-11 10 μ F capacitors on the 1.5 V or 1.8 V power paths (1)

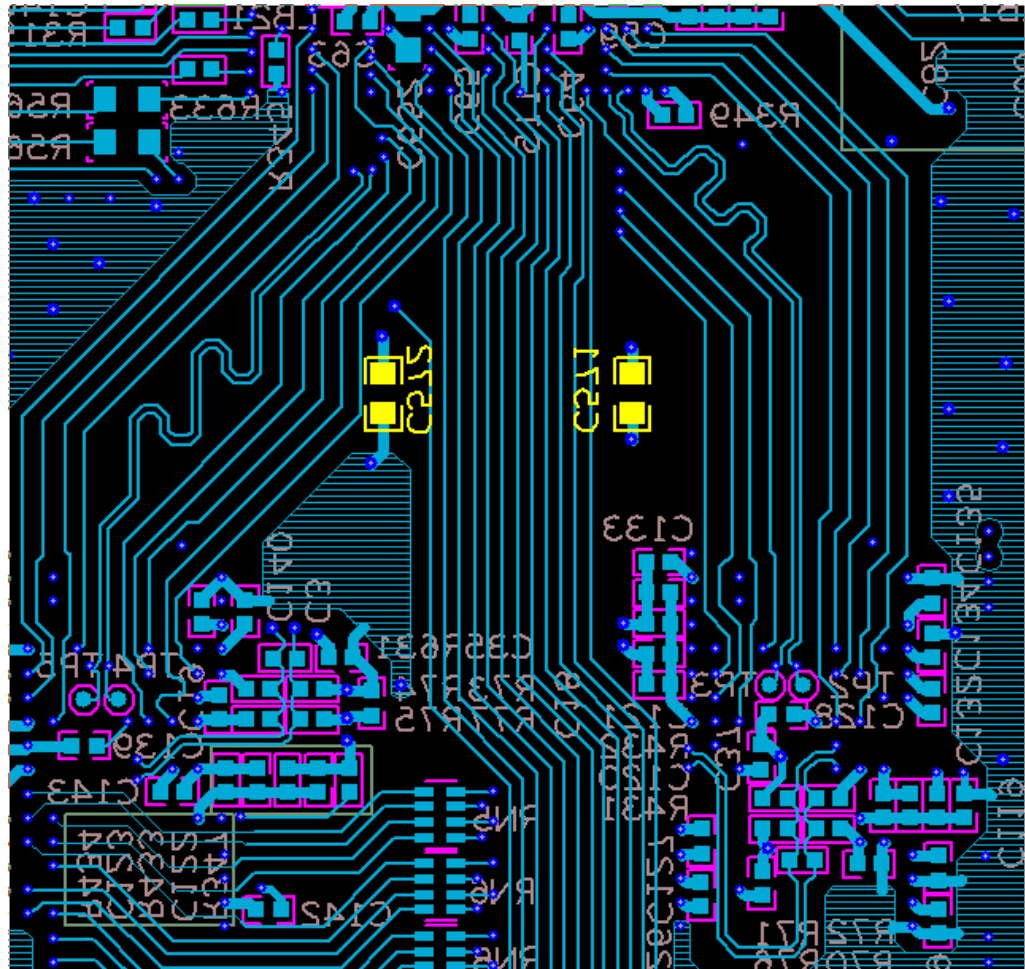
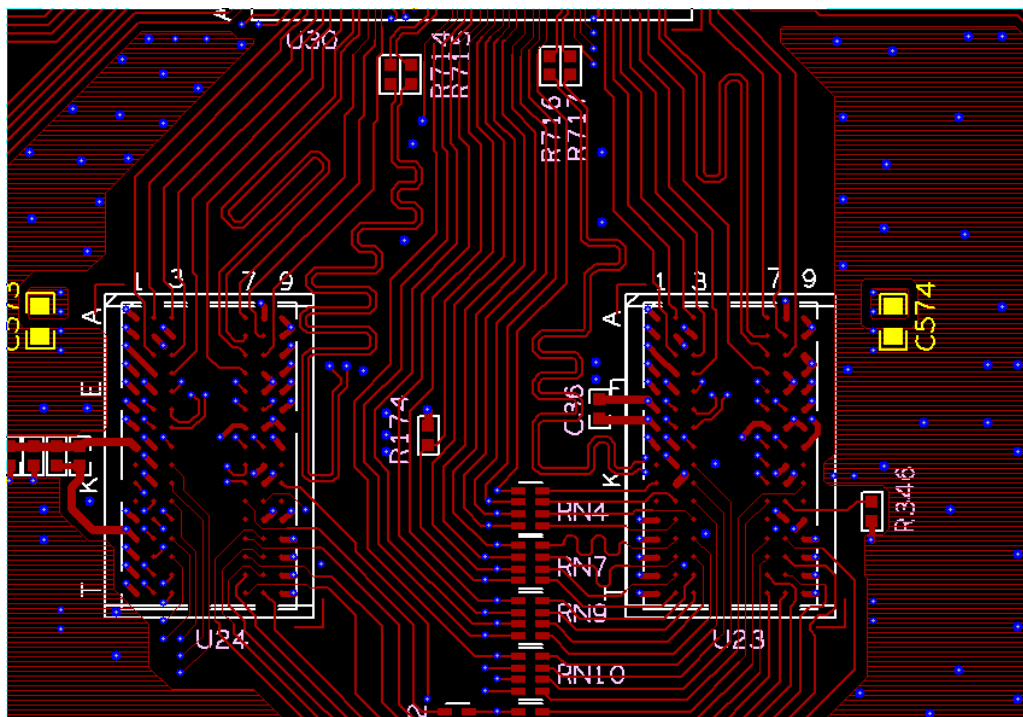


Figure 2-12 10 μ F capacitors on the 1.5 V or 1.8 V power paths (2)



The recommendations for designing the VREF are as follows:

- Pay attention to the VREF routing when designing the VREF. According to the SSTL-15 standard, the noise of the VREF cannot be greater than $\pm 1\%$ of the VREF level. To reduce the noise, the VREF traces should be as wide as possible. It is recommended to route the VREF traces at the power layer over a copper plane. This plane cannot be used as the reference plane for routing signal traces.
- A decoupling capacitor needs to be connected to each VREF pin. The trace of each VREF pin should be as wide as possible and the spacing between the trace and other signal traces must be 20–25 mils.

2.3.2 Signal Design



NOTE

This section describes the signal design by using the 16-bit DDR3 as an example.

Ensure that DDR traces have the same length by taking on-chip trace lengths into account. See [Table 2-1](#).

Table 2-1 DDR on-chip trace lengths

Net Name	On-Chip Trace Length (Mil)	Net Name	On-Chip Trace Length (Mil)
DDR_A0	225.6098425	DDR_DQ10	233.2862205
DDR_A1	135.1224409	DDR_DQ11	273.3224409



Net Name	On-Chip Trace Length (Mil)	Net Name	On-Chip Trace Length (Mil)
DDR_A2	155.6885827	DDR_DQ12	292.5507874
DDR_A3	195.5511811	DDR_DQ13	261.5366142
DDR_A4	144.3472441	DDR_DQ14	296.1649606
DDR_A5	217.8531496	DDR_DQ15	279.0480315
DDR_A6	134.465748	DDR_DQ16	251.0188976
DDR_A7	210.0173228	DDR_DQ17	170.5472441
DDR_A8	98.94685039	DDR_DQ18	202.2204724
DDR_A9	188.9177165	DDR_DQ19	277.8787402
DDR_A10	134.7051181	DDR_DQ20	112.9492126
DDR_A11	115.8318898	DDR_DQ21	182.8795276
DDR_A12	112.4708661	DDR_DQ22	202.3322835
DDR_A13	207.6877953	DDR_DQ23	188.3791339
DDR_A14	104.6590551	DDR_DQ24	293.6858268
DDR_BA0	237.1031496	DDR_DQ25	287.6338583
DDR_BA1	187.6759843	DDR_DQ26	265.5625984
DDR_BA2	225.6641732	DDR_DQ27	308.2818898
DDR_CAS_N	180.7125984	DDR_DQ28	271.9598425
DDR_CKE	130.4212598	DDR_DQ29	293.0389764
DDR_CLK0_N	223.6885827	DDR_DQ30	317.034252
DDR_CLK0_P	227.4688976	DDR_DQ31	279.8259843
DDR_CLK1_N	253.353937	DDR_DQS0_N	216.6614173



Net Name	On-Chip Trace Length (Mil)	Net Name	On-Chip Trace Length (Mil)
DDR_CLK1_P	256.8681102	DDR_DQS0_P	220.146063
DDR_CS_N	199.0137795	DDR_DQS1_N	254.4322835
DDR_DM0	113.2350394	DDR_DQS1_P	272.1767717
DDR_DM1	290.7637795	DDR_DQS2_N	267.1059055
DDR_DM2	148.711811	DDR_DQS2_P	270.9251969
DDR_DM3	242.0535433	DDR_DQS3_N	342.8385827
DDR_DQ0	225.4031496	DDR_DQS3_P	339.1653543
DDR_DQ1	173.5358268	DDR_ODT	266.3854331
DDR_DQ2	239.230315	DDR_PADHI	187.6555118
DDR_DQ3	140.4728346	DDR_PADLO	238.7354331
DDR_DQ4	157.6220472	DDR_RAS_N	197.426378
DDR_DQ5	172.538189	DDR_REF	241.2240157
DDR_DQ6	133.8622047	DDR_RESET_N	231.2448819
DDR_DQ7	150.4066929	DDR_RTT	161.1582677
DDR_DQ8	265.1944882	DDR_WE_N	208.8507874
DDR_DQ9	255.7858268		

Clock Signal CLK

The requirements on the length of the clock signal CLK are as follows:

- The maximum trace length of the CLK signal must be less than or equal to 4 inches.
- The CLK differential signals must be routed based on the traces of the differential signals and the deviation of each pair of differential traces is less than 5 mils. That is, the following condition must be met: $|LCLKxP - LCLKxN| < 5$ mils.
- The width and spacing of the DDR trace cannot be less than 4 mils. The impedance of the CLK differential trace must be within 100 Ω .



DQS Signal

For DQS traces, the requirements are as follows:

- The lengths of the two internal DQS differential signal traces must be the same and the deviation of each pair of differential traces is less than 5 mils. That is, the following condition must be met: $|LDQS \times P - LDQS \times N| < 5$ mils.
- DQS traces are routed based on the length of the CLK traces. The deviation of the DQS is ± 1100 mils relative to the trace length of the CLK. That is, $LDQSx = LCLKx \pm 1100$ mils.
- The impedance of the DQS differential trace must be within 100Ω .

Data Signals DQ[0:31]

The data signals DQ[31:0] are routed based on the trace length of the DQS and the length deviation is ± 300 mils. The details are as follows:

- DQ[7:0] are routed based on the length of the DQS0 trace and the length deviation is ± 300 mils. That is, $LDQ[7:0] = LDQS0 \pm 300$ mils.
- DQ[15:8] are routed based on the length of the DQS1 trace and the length deviation is ± 300 mils. That is, $LDQ[15:8] = LDQS1 \pm 300$ mils.
- DQ[23:16] are routed based on the length of the DQS2 trace and the length deviation is ± 300 mils. That is, $LDQ[23:16] = LDQS2 \pm 300$ mils.
- DQ[31:24] are routed based on the length of the DQS3 trace and the length deviation is ± 300 mils. That is, $LDQ[31:24] = LDQS3 \pm 300$ mils.
- It is recommended that the GND layer is the reference plane of the data trace. If no reference plane is available, the traces of the same group must be routed at the same layer.

Data Mask Signal DM

The data mask signal DM is routed based on the trace length of the DQS. The requirements are as follows:

- DM0 is routed based on the length of DQS0 trace and the length deviation is ± 300 mils.
- DM1 is routed based on the length of DQS1 trace and the length deviation is ± 300 mils.
- DM2 is routed based on the length of DQS2 trace and the length deviation is ± 300 mils.
- DM3 is routed based on the length of DQS3 trace and the length deviation is ± 300 mils.

Address Signals ADDR[0:14]

For the address signal trace ADDR[0:14], the requirements are as follows:

- ADDR[0:14] are routed based on the trace length of the CLK and the length deviation is $+500$ mils or -1000 mils. That is, $LADDR = LCLK + 500$ mils or $LADDR = LCLK - 1000$ mils.
- The address trace uses the T-shaped trace. The maximum trace length from the T point to the Hi3521 pin is 2 inches. The maximum trace length from the T point to a DDR is 1 inch, and one 22Ω resistor must be connected in series between the T point to each DDR.
- On the same network, the length difference between the trace from a T point to the left DDR and the trace from the T point to the right DDR is within 300 mils.



Control Signals

For the control signal traces including BA[0:2], DM, CKE, CSN, WEN, CASN, RASN, and ODT, the requirements on control signal traces and address signal traces are the same. For details, see the description of address signal traces.

PCB Routing Recommendations

Route traces on a PCB according to the following guidelines:



CAUTION

The routing design for the DDR must be the same as that for the Hi3521 demo board. If you cannot use such design, comply with the following guidelines and send design documents to HiSilicon field application engineers (FAEs).

- Never cross the power or GND plane splits when routing DDR3 SDRAM traces, and route all DDR signal traces by referring to a complete plane.
- The characteristic impedance must be $50\ \Omega \pm 10\%$ for each single-end signal trace and $100\ \Omega \pm 10\%$ for each differential trace.
- The DQ signal traces in the same group must be routed at the same layer. A DQ signal group has 11 signal traces, including 8-bit DQx signals, a DMx signal, and a pair of DQSx differential signals. The signal traces in the same group must be routed at the same layer by referring to the same current return plane.
- The DQ and DM signals of the chip can connect to those of the DDR by using straight traces. In this case, the spacing between adjacent traces must be four times the trace width, which is called 4W rule. See [Figure 2-13](#). The snake-shape traces can also be used.
- The address signal traces A[X] and control signal traces must meet length requirements and are as short as possible. The spacing between adjacent spaces must be three times the trace width, which is called 3W rule.
- Most clock signal traces CLK must be routed at the top layer, and vias are punched around the DDR and connected to the Thevenin equivalent resistors at the bottom layer, as shown in [Figure 2-13](#). In addition, one 100 nF filtering capacitor connects to the 1.5 V power for the Thevenin equivalent resistors, as shown in [Figure 2-14](#).



Figure 2-13 Clock signal trace routing

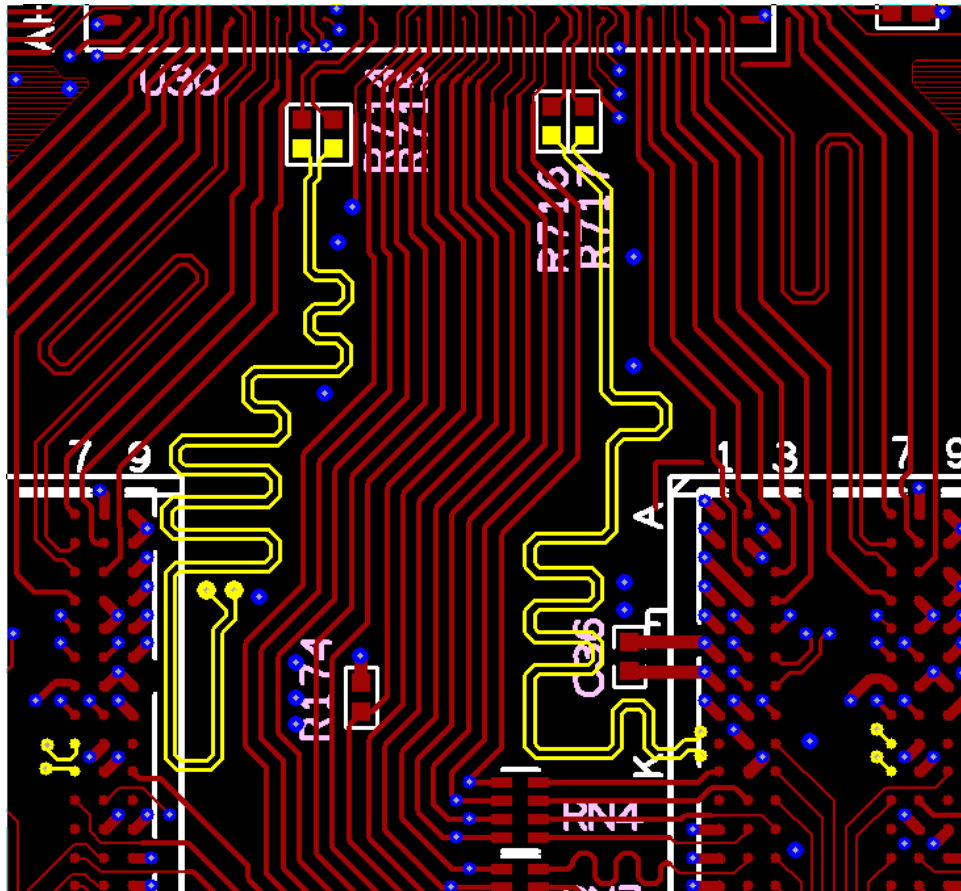
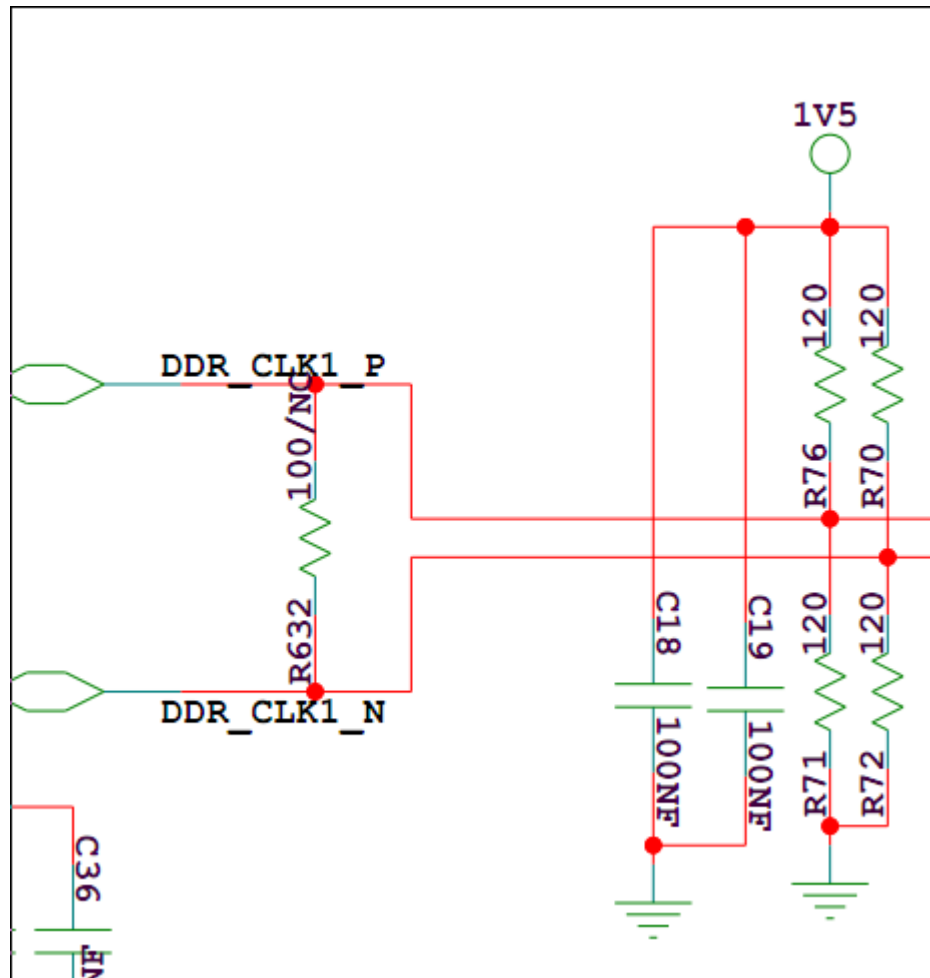
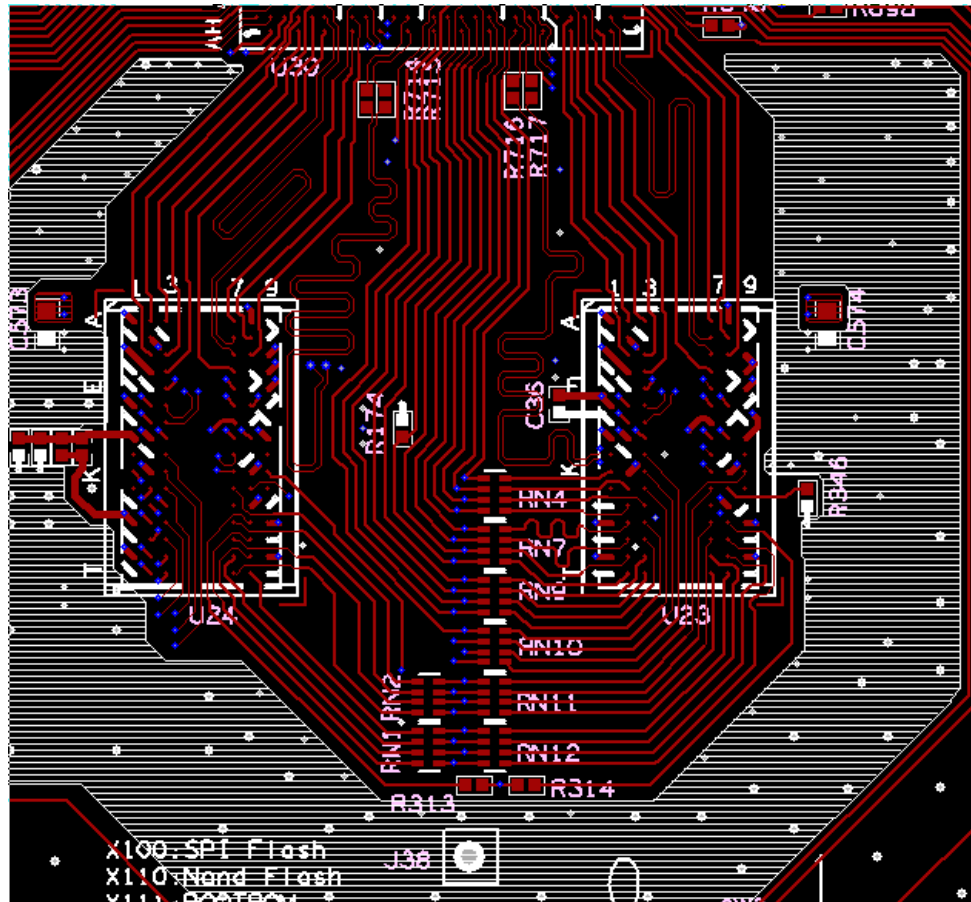


Figure 2-14 Filtering capacitor connected to the 1.5 V power for the Thevenin equivalent resistors



- The space between a DDR3 SDRAM trace and other signal traces must be at least 20 mils, and the DDR3 SDRAM traces are surrounded with GND traces, as shown in [Figure 2-15](#).

Figure 2-15 DDR surrounded with GND traces



- One decoupling capacitor connects to each VREF pin. The trace of each VREF pin must be as wide as possible, and the recommended spacing between the VREF pin trace and other signal traces is greater than 20 mils.

2.4 Design Recommendations for the GMAC Traces

As the rate of GMAC signals is high, you are advised to design the PCB routing according to the following requirements to reduce signal crosstalk:

- Avoid routing signal traces across power plane splits and keep complete reference planes for signal traces.
- Determine the signal trace length based on the clock trace length, and ensure that the length deviation is ± 200 mils.
- The GND under the transformer chip is void.
- Each pair of differential traces (MDI+₀, MDI-₀, MDI+₁, MDI-₁, MDI+₂, MDI-₂, MDI+₃, and MDI-₃) has the same length, the length deviation is ± 5 mils, and the impedance of each differential trace is $100\ \Omega \pm 10\%$.



2.5 Design Recommendations for the Circuit of the USB Port

To ensure good signal quality, the data traces of the USB 2.0 host port must be routed in differential mode. To match the 480 MHz/s USB 2.0 port, you are advised to design the PCB routing according to the following guidelines:

- The differential data traces must be short and straight and the internal differential traces must have the same length. It is recommended that the trace deviation is within 5 mils.
- The impedance of each differential data trace is $90\ \Omega \pm 10\%$.
- Route differential data traces on the plane that is close to the ground plane and never change the routing plane.
- Route differential data traces by referencing complete ground planes and do not cross the plane splits.
- Minimize the use of vias and corners when routing differential data traces. When corners are required, use arcs or 135° turns rather than a 90° turn. This reduces the signal reflection and impedance variance.
- Keep the differential data traces away from other high-speed cyclic signal traces and large current signal traces. The spacing must be greater than 50 mils. In this way, the crosstalk effect is reduced. In addition, keep the differential data traces away from the low-speed non-cyclic signals and ensure that the spacing is at least 20 mils.
- Place the REXT resistor close to the Hi3521.

2.6 Design Recommendations for the SATA Traces

The Hi3521 provides two SATA interfaces. The trace recommendations are as follows:

- The differential impedance of the SATA traces must be within $100\ \Omega \pm 10\%$.
- The 10 nF SMT capacitor connected in series on the differential signal trace must be placed close to the SATA socket.
- The recommended signal trace length on the PCB is less than 5 inches.

2.7 Design Recommendations for the HDMI Traces

The Hi3521 has an HDMI interface that outputs HDMI signals directly. The trace recommendations are as follows:

- The differential impedance of the four pairs of HDMI differential signals must be within $100\ \Omega \pm 10\%$.
- The ESD components must be placed close to the HDMI socket.
- It is recommended that the signal trace at the corners should be arcs as much as possible.
- The recommended length of four pairs of HDMI differential signal traces is shorter than 3.5 inches.



2.8 Design Recommendations for the VI and VO Traces

The Hi3521 has two BT.1120 input interfaces and each of them can be multiplexed as two BT.656 interfaces. The trace recommendations are as follows:

- When the BT.1120 interfaces are used, the data traces, horizontal sync signal traces, and vertical sync signal traces are routed based on the length of the CLK signal. The recommended deviation length is within 100 mils.
- When each of the BT.1120 interfaces is divided into two BT.656 interfaces, the upper eight-bit data traces are routed based on the length of the CLK signal of the BT.1120. The recommended deviation is within 100 mils. The lower eight-bit data traces are routed based on the vertical sync signal traces of the BT.1120. The horizontal sync signal is multiplexed as the sampling clock signal of the lower eight-bit data trace. The recommended deviation is within 100 mils.

2.9 Design Recommendations for the Traces of the System and Peripheral Reset Signals

To ensure that the system and peripheral reset signal traces are not interfered, you are advised to route them far away from other signals especially high-speed digital signal traces. To be specific, the reset signal traces must be at least three times of trace wide away from high-speed digital signal traces.

2.10 Design Recommendations for PCIe Pins

The Hi3521 does not support the peripheral component interconnect express (PCIe) function. The Hi3521 PCIe pins are reserved for expansion. Pay attention to the connection modes for the PCIe pins. See [Table 2-2](#).

Table 2-2 Connection modes for PCIe pins

Pin Name	Connection Mode
PCIE_RXP	Floated
PCIE_RXM	Floated
PCIE_TXP	Floated
PCIE_TXM	Floated
PCIE_REFCLKP	Floated
PCIE_REFCLKM	Floated
PCIE_VPH25	Connect this pin to the power supply and keep the power supply on.
PCIE_VP10	Connect this pin to the power supply and keep the power supply on.
PCIE_REXT	Connect this pin to a 1% 191 Ω resistor and then to GND.



2.11 Design Recommendations for the System Power and Ground



CAUTION

If the minimum system design for the Hi3521 demo board is not applicable, send your own design documents to field application engineers (FAEs) for review.

The design recommendations for the system power supply are as follows:

- The minimum system design for the Hi3521 demo board (including the fanout mode and filtering capacitor layout) is recommended.
- It is recommended that the width of the 1.0 V power can bear the overcurrent of 5 A or larger.
- The 1.5 V or 1.8 V power supply of the DDR interface and the DDR2 or DDR3 power supply share a power plane.
- The PLL GND is not connected to the system GND directly. Instead, the PLL GND is connected over a single point.
- All 3.3 V power supplies of the peripherals share a power plane.
- Ensure the integrity of the GND at the top layer and the bottom layer. This helps heat dissipation and electronic magnetic interface (EMI) suppression.

2.12 Design Recommendations for the Integrity Simulation of PCB Signals

By using the board-level simulation tools, the PCB designers can simulate signals and analyze signal integrity based on the input/output buffer information specification (IBIS) models of the Hi3521 interfaces, IBIS models of components, transmission line models, and board topologies.

Based on the simulation results, the PCB designers can adjust the typologies to meet the signal quality requirements, such as the requirements for overshoot, undershoot, ringtone, and monotonicity.



3

Design Recommendations for the Board Heat Dissipation

3.1 Working Condition

For details about power supply parameters, temperature parameters, and thermal resistance parameters for the Hi3521/Hi3520A, see section 2.6 "Electrical Specifications" in the *Hi3521/Hi3520A H.264 Codec Processor Data Sheet*.

3.2 Heat Dissipation Design Reference

Heat Sink Specifications

The thermal resistance of the components and heat sinks must meet the following condition:

$$\theta_{sa} < (T_{j_max} - T_a)/P - \theta_{jc} - \theta_{cs}$$

where

- T_{j_max} is the maximum junction temperature of a component.
- P is power consumption.
- T_a is the maximum ambient temperature.
- θ_{jc} is the junction-to-case thermal resistance of a component.
- θ_{cs} is the thermal resistance between a component and a heat sink.

For the Hi3521, the 31 mm x 31 mm x 16 mm (1.22 in. x 1.22 in. x 0.63 in.) heat sink is required. The dimensions of the heat sink rack are 1.0 mm x 1.5 mm x 13 mm (0.04 in. x 0.06 in. x 0.51 in.). You are advised to paint the heat sink surface black, and select the recommended heat sink or another one with better performance. Apply thermally conductive silicone to the contact surface between the heat sink and the Hi3521. In addition, install insulation gaskets as required. See [Figure 3-1](#).

Figure 3-1 Heat sink

NOTE

The preceding specifications are only for reference. You need to select heat sinks based on the board design.

Recommended Thermally Conductive Materials

[Table 3-1](#) describes recommended thermally conductive materials.

Table 3-1 Recommended thermally conductive materials

Mode of Fixing Heat Sinks	Model	Thermally Conductive Coefficient (w/m k)	Ambient Temperature (°C)	Colloid Type	Insulation Strength (V/mil)	Flame Resistance	Bearing Capacity (g)
Mechanical fixing	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Non-mechanical fixing	Locotite 315	0.808	N/A	Acrylic resin	6000	UL9V2	N/A

Relationship Between the Fixing Mode and the Heat Sink Mass

The fixing mode of the heat sink depends on the heat sink mass. You are advised not to fix a large-mass heat sink by using the thermally conductive adhesive. [Table 3-2](#) describes the relationship between the fixing mode and the heat sink mass. You can select the fixing mode based on the board design.



Table 3-2 Relationship between the fixing mode and the heat sink mass

Fixing Mode	Mass		
	$m < 85\text{ g}$	$85 \leq m < 150\text{ g}$	$m \geq 150\text{ g}$
Thermally conductive adhesive	√	×	×
Push-pin buckle	√	×	×
Spring and screw	×	√	√
Dedicated metal buckle (non-preferable)	√	√	√
Plastic holder (non-preferable)	√	×	×

3.3 Reference Design for Circuit Heat Dissipation

3.3.1 Schematic Diagram

Power Supply

Ensure that the efficiency of the board power tree is highest as long as the power supply is stable. That is, you design the board power supply optimally and use fewer LDO components with large voltage difference. This reduces the heat produced during power supply conversion.

The board provides power supplies for peripherals such as the SD card and USB device. During design, you can shut down such power supplies when they are not used. The main ICs of the board must support the power-down mode.

Low-Power Configurations for Idle Modules

In the actual application, the modules such as the VO module, USB module, and SATA module may not be used. In this case, you can set the mode of these modules to power-down mode or default mode.



CAUTION

Enable clock gating for the main chip to reduce power consumption.



3.3.2 PCB

Component Layout

Lay out components as follows based on the product architecture and heat dissipation design:

- Place the components that consume much power and generate much heat in a distributed manner to avoid overheating of some parts and ensure the reliability and efficiency of components. In addition, you are advised to place the Hi3521 away from power supplies.
- Design the product architecture optimally to ensure that the heat produced internally can be dissipated.

Routing

The routing recommendations are as follows:

- For the connection style of the vias under the Hi3521, select the full connection style rather than the thermal connection style to improve the dissipation efficiency of the board.
- Connect the GND signals and 1.0 V, 1.5 V (or 1.8 V), and 3.3 V power signals over copper planes. When the signal overcurrent performance is ensured, you are advised to punch more vias and then connect these vias to copper planes.
- Increase the size of copper planes under and around the components that produce much heat to ensure that the heat of the PCB can be dissipated effectively. For the inductors and power chips, place them in a distributed manner and increase the size of copper planes around them.